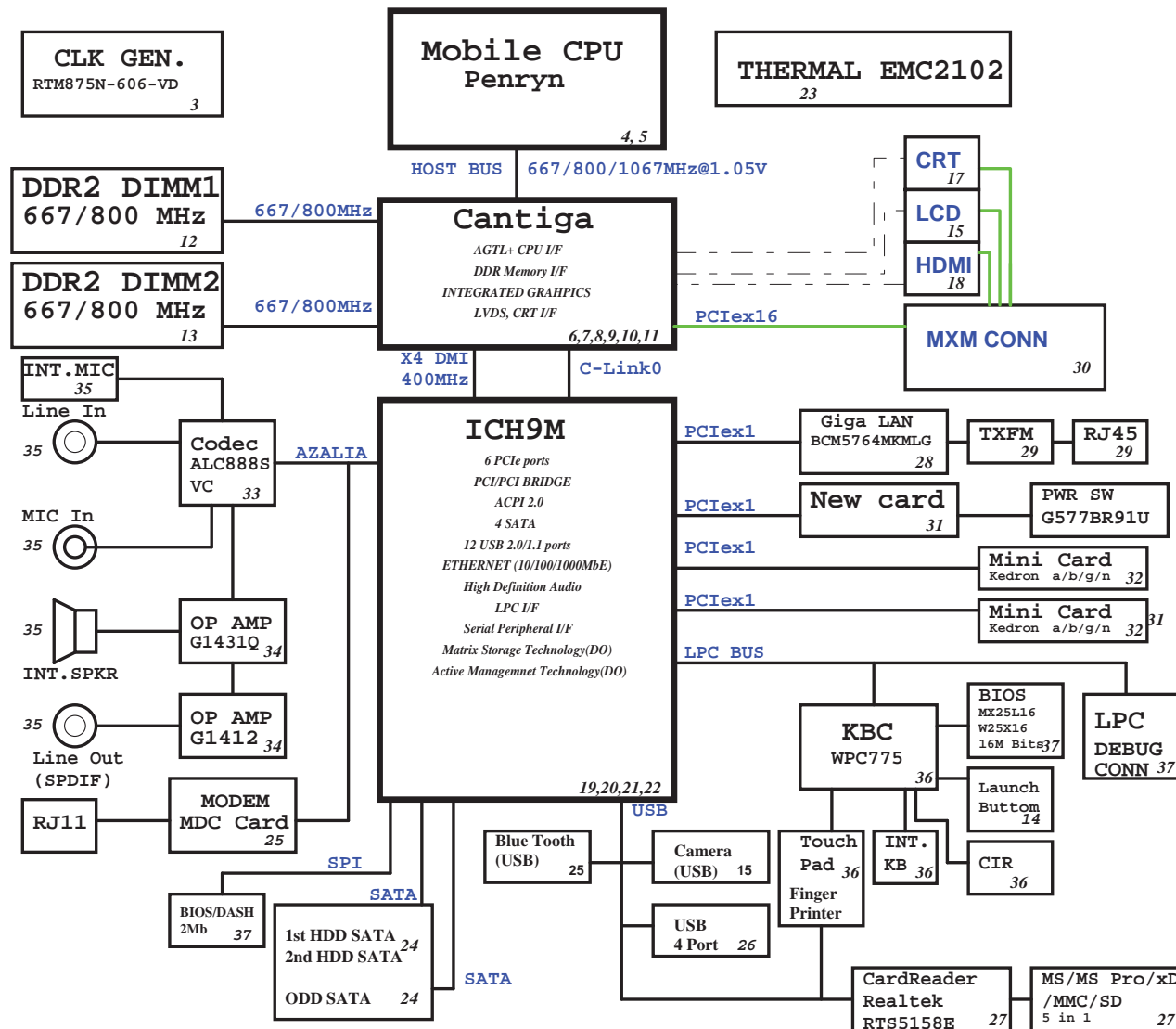


Big Bear 2 Block Diagram

Project code: 91.4AV01.001
PCB P/N : 48.4AV01.
REVISION : -1



PCB STACKUP

TOP	_____
VCC	=====
S	_____
S	_____
GND	=====
BOTTOM	_____

SYSTEM DC/DC	
TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC	
TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3
RT9018A 44	
1D8V_S3	1D5V_S0
G9131 44	
3D3V_S0	2D5V_S0
GFXCORE DC/DC	
ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7-1.25V
CPU DC/DC	
ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35-1.5V
CHARGER	
BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
BLOCK DIAGRAM			
Size	Document Number	Rev	
Custom	Big Bear 2	-1	
Date: Wednesday, October 22, 2008		Sheet 1	of 50

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

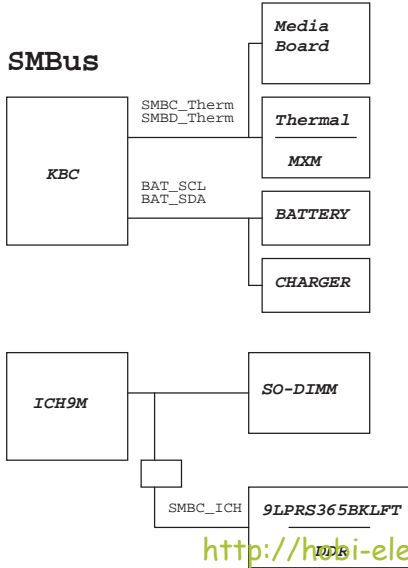
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	NC

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	USB5(DOCK)
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

SMBus



ICH9M Integrated Pull-up
and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS1PVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller
Hub strapping configuration

Montevina Platform Design guide 22339 0.5
page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

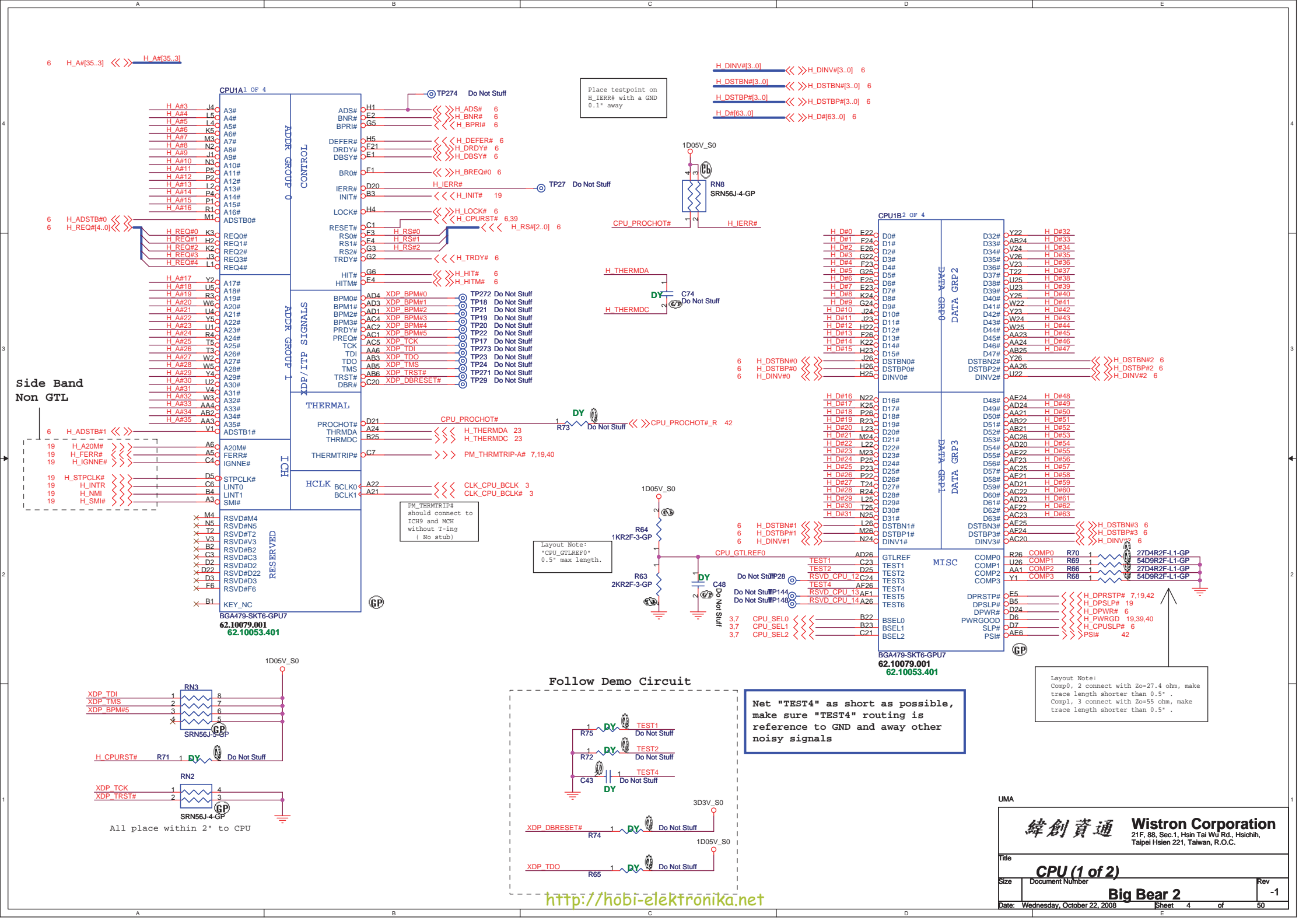
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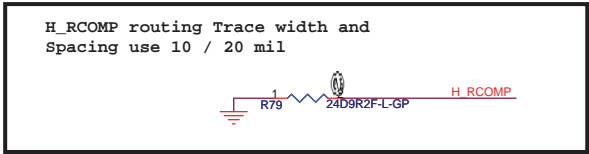
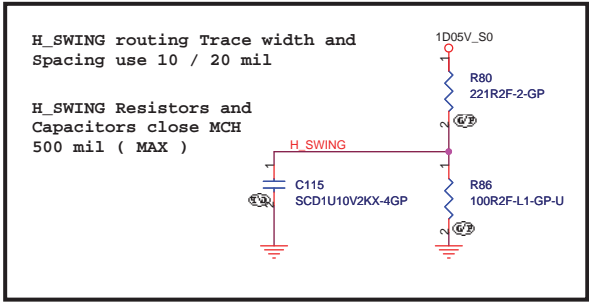
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

UMA

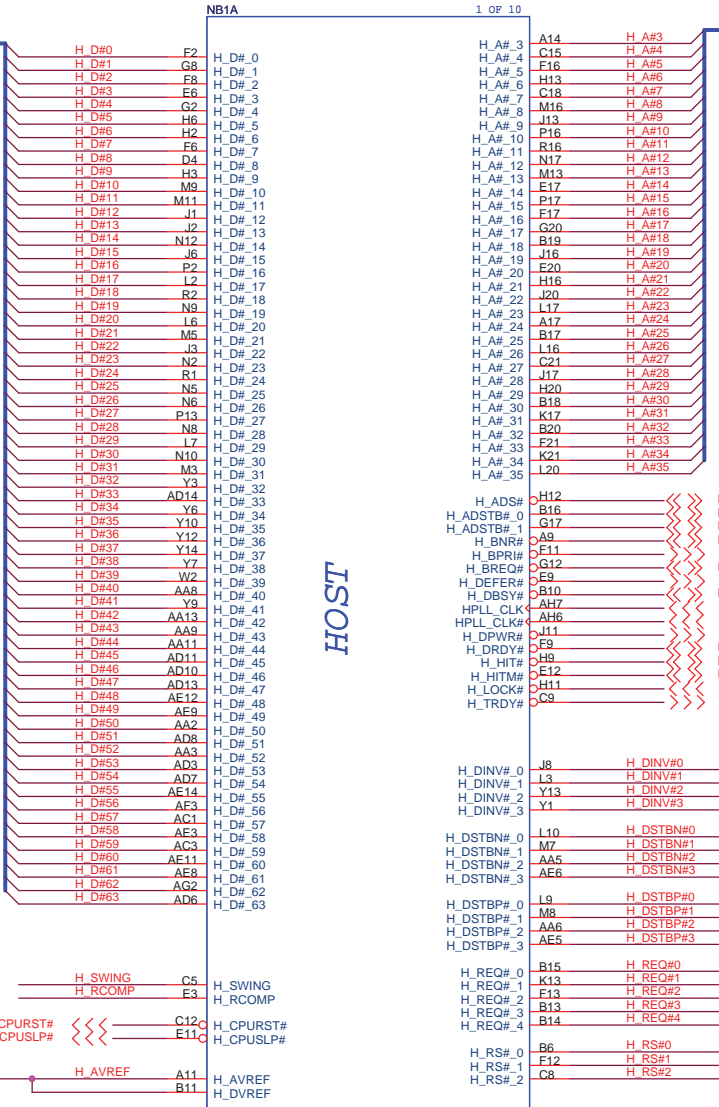
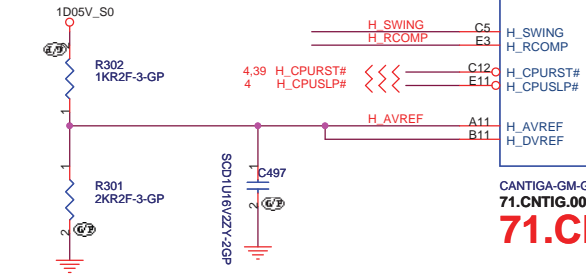
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number
Big Bear 2	
Date: Wednesday, October 22, 2008	Sheet 2 of 50
Rev -1	

<http://hbi-elektronika.net>



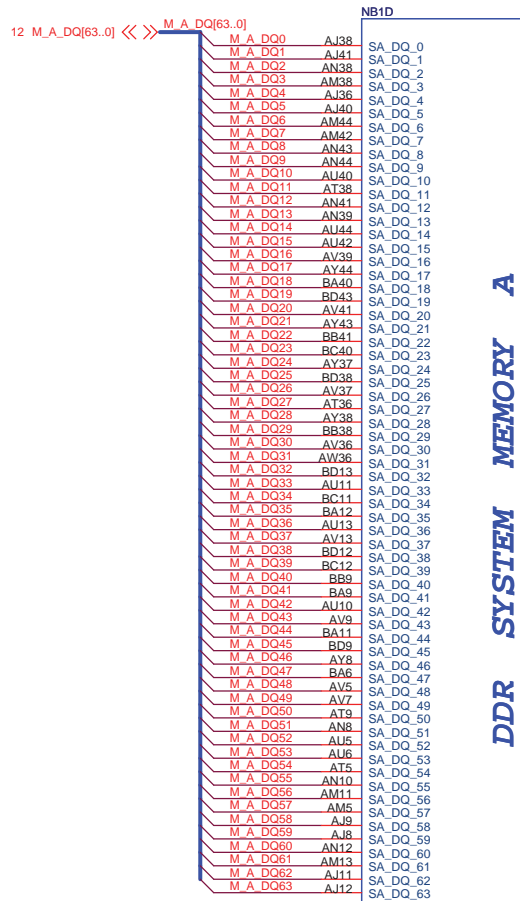


Place them near to the chip (< 0.5")

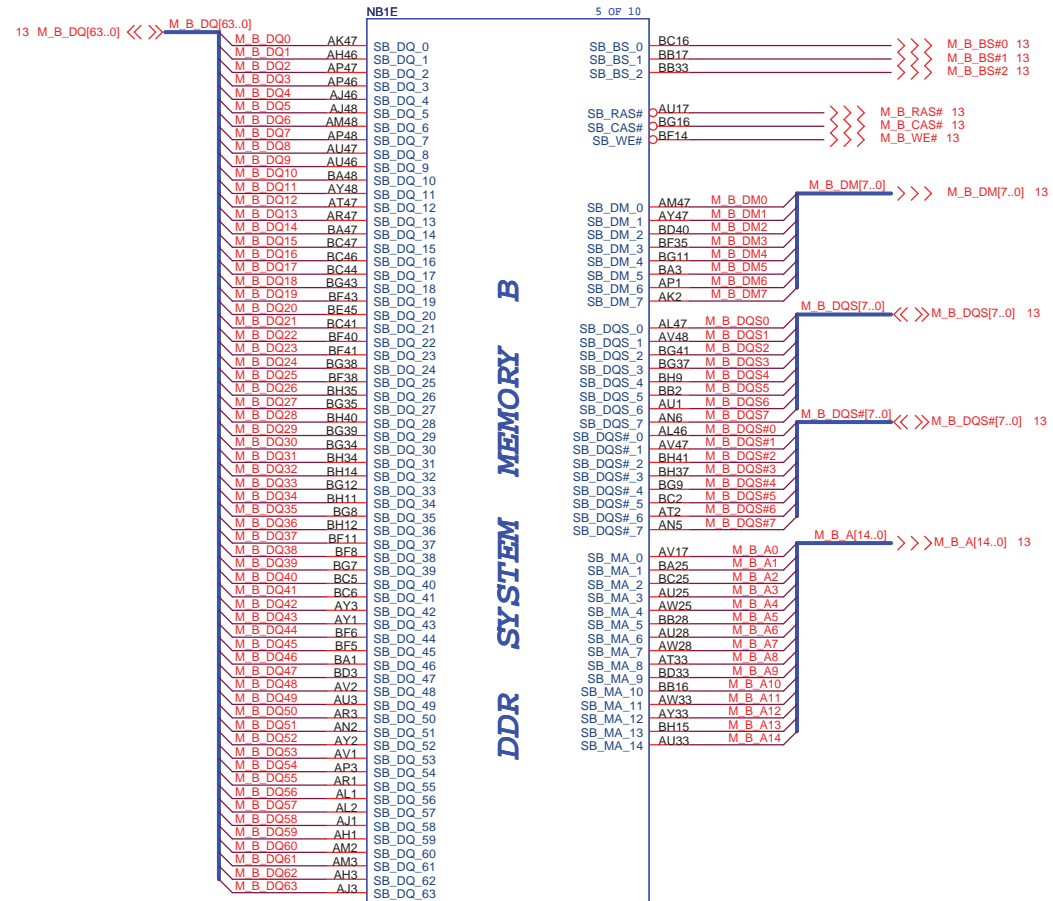


CANTIGA-GM-GP-U-NF
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71.CNTIG.D1U

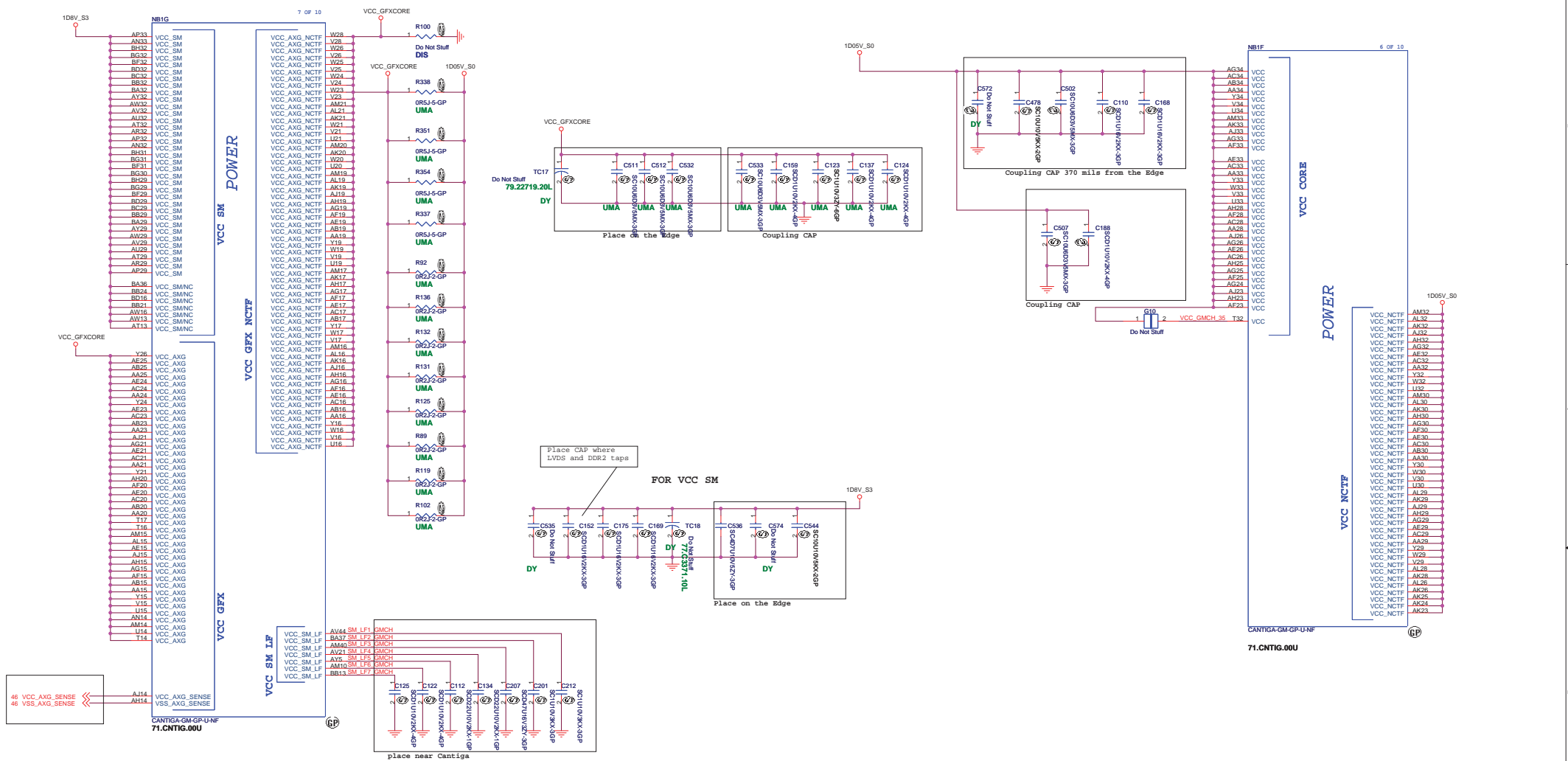




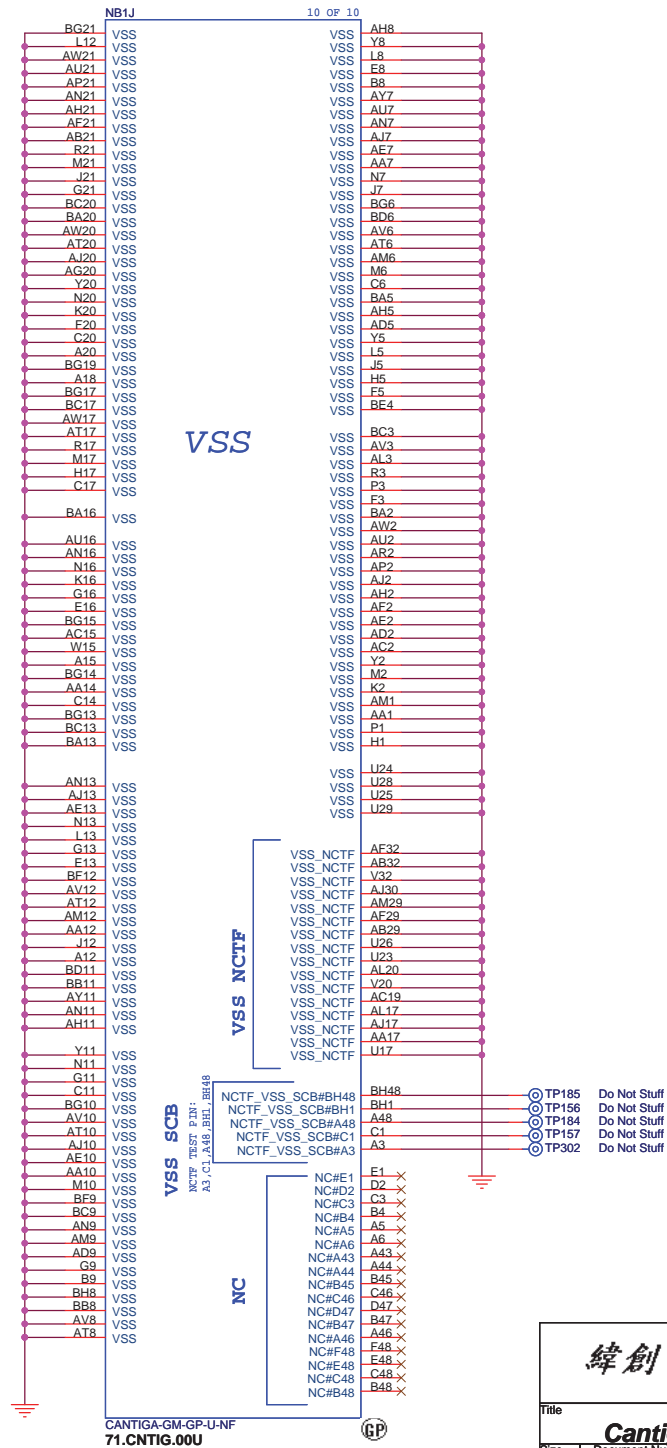
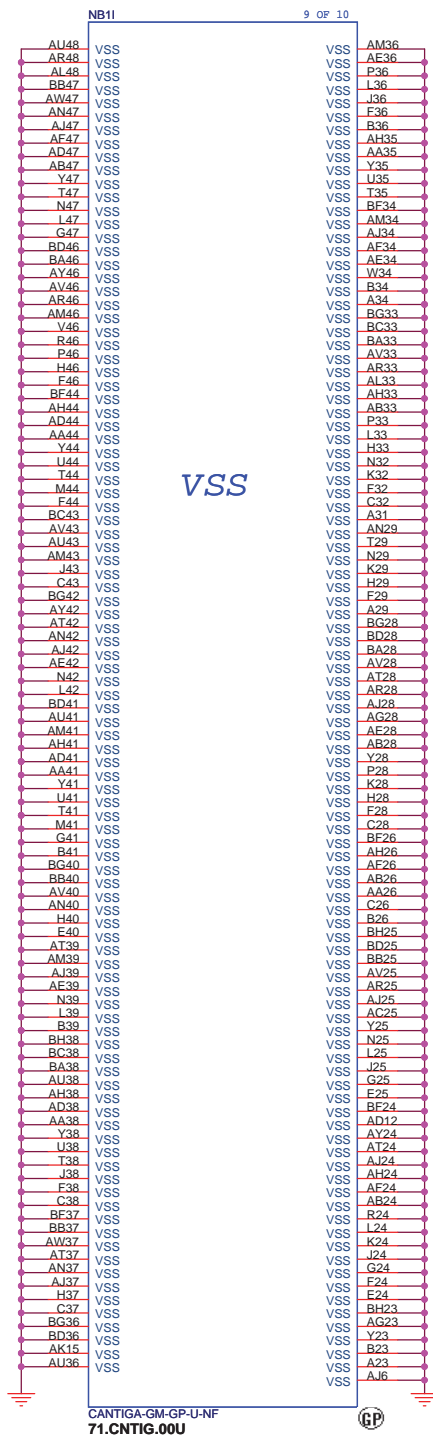
CANTIGA-GM-GP-U-NF
71.CNTIG.00U



CANTIGA-GM-GP-U-NF
71.CNTIG.00U







PARALLEL TERMINA

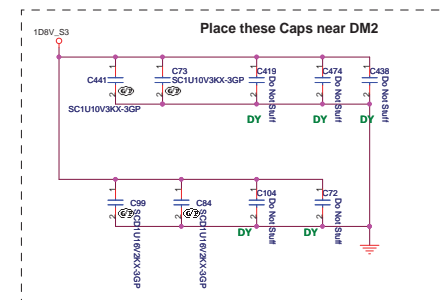
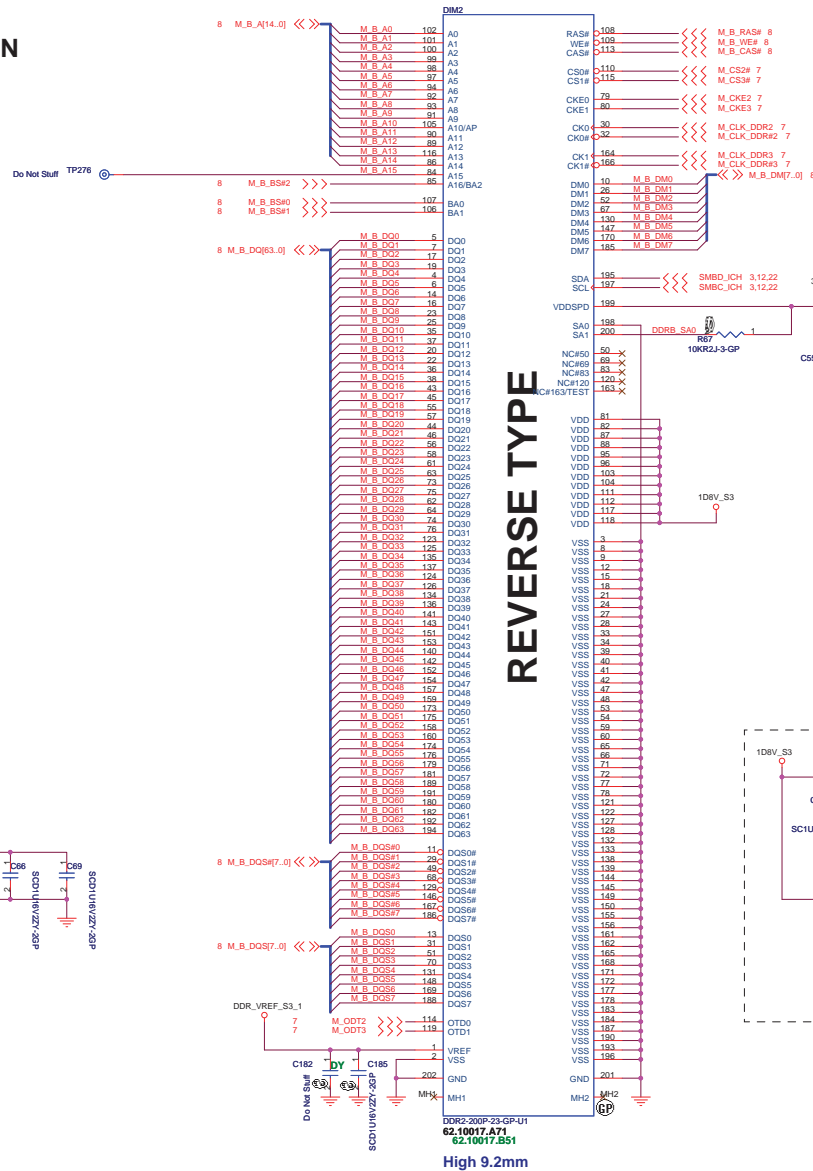
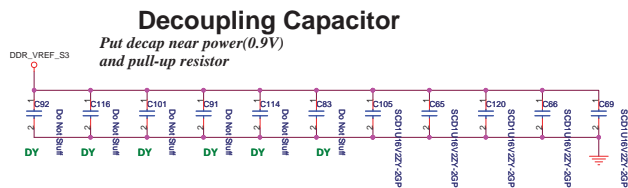
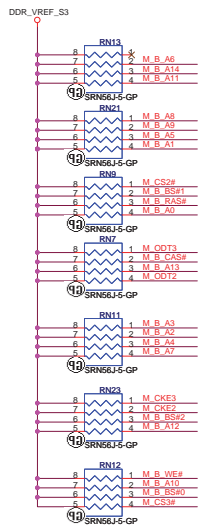
Put decap near power(0.9V) and pull-up resistor

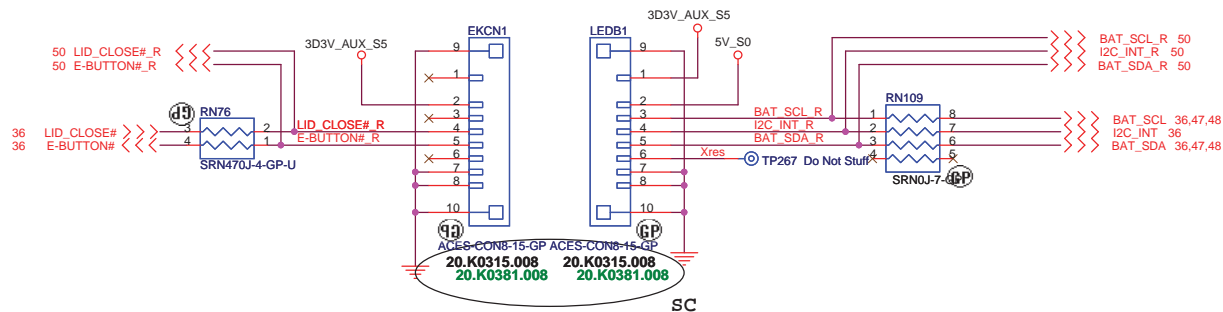
The diagram shows a parallel bus termination circuit. The bus is connected to VREF_S3 and has a pull-up resistor of 10k. The bus lines are terminated with 50 ohm resistors (RN2, RN10, RN20, RN75, RN81, RN22, RN77) and connected to various memory chips (M_A A9, M_A A12, M_A BSF2, M_CKE0, M_A A13, M_CS0B, M_ODT0, M_A DAS2, M_A BS41, M_A A0, M_A A2, M_A A4, M_ODT1, M_CS1B, M_A CAS9, M_A A3, M_A A14, M_A A5, M_A A6, M_CKE1, M_A A11, M_A A7, M_A A6, M_CKE1, M_A WE4, M_A BS40, M_A A10, M_A A1). The bus is labeled 10 and the termination resistors are labeled 50.

Put decap near power (0.9V) and pull-up resistor

The diagram shows a horizontal power plane for 0.9V. It includes a pull-up resistor labeled 'D0R_VREF_S3' at the top left. A series of decoupling capacitors are placed along the plane, labeled C421, C427, C432, C107, C265, C70, C424, C470, C439, and C463. Each capacitor is connected to a specific net: #D5, #D6, #D7, #D8, #D9, #D10, #D11, #D12, #D13, and #D14. The capacitors are represented by two parallel lines for the plates. The nets are labeled with their respective designators: D5, D6, D7, D8, D9, D10, D11, D12, D13, and D14. The ground connection is shown at the bottom right.

[illegible][illegible]





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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAUNCH

Size	Document Number
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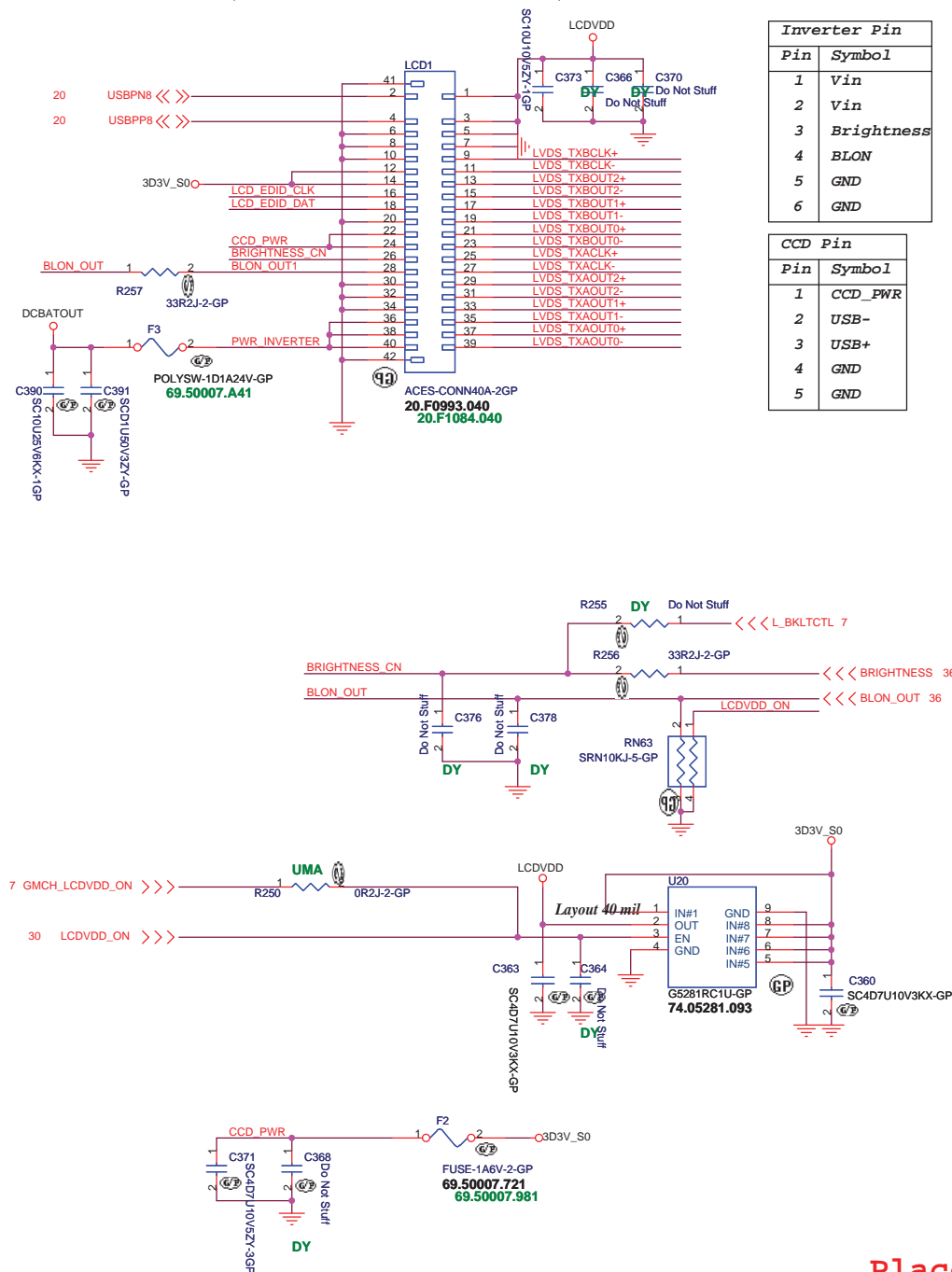
Big Bear 2

Rev
-1

Date: Wednesday, October 22, 2008

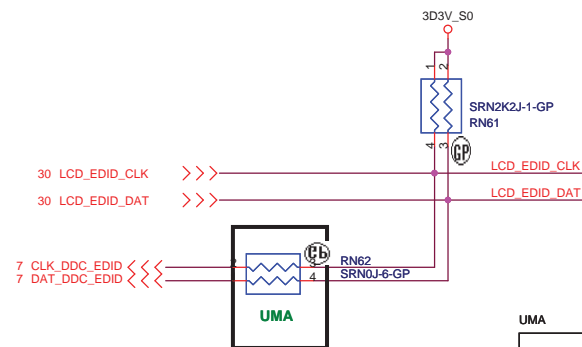
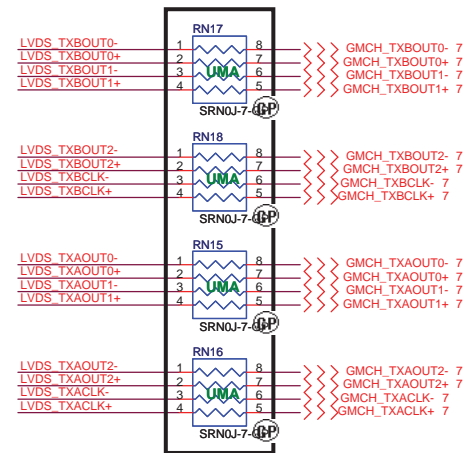
Sheet 14 of 50

Place close to MXM slot for BB2



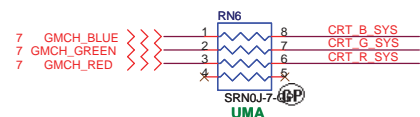
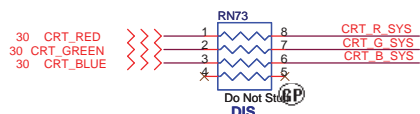
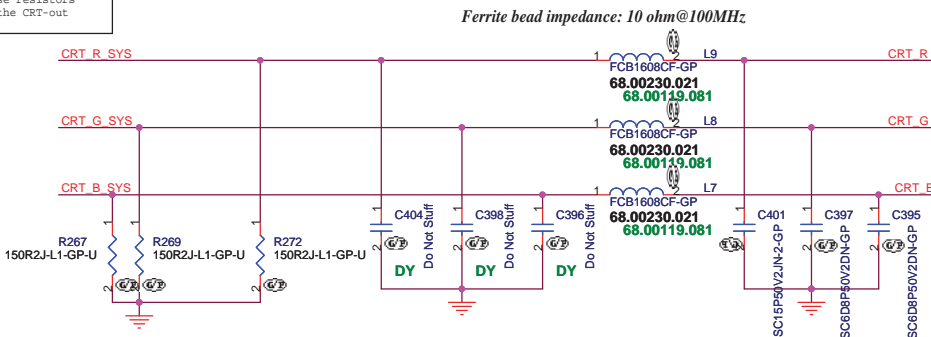
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



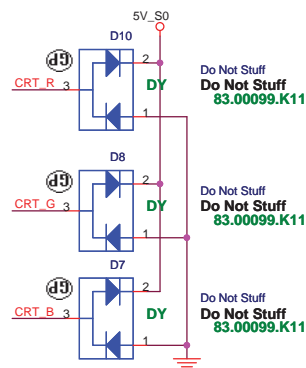
Place close to MXM slot for BB2

Layout Note:
Place these resistors
close to the CRT-out
connector

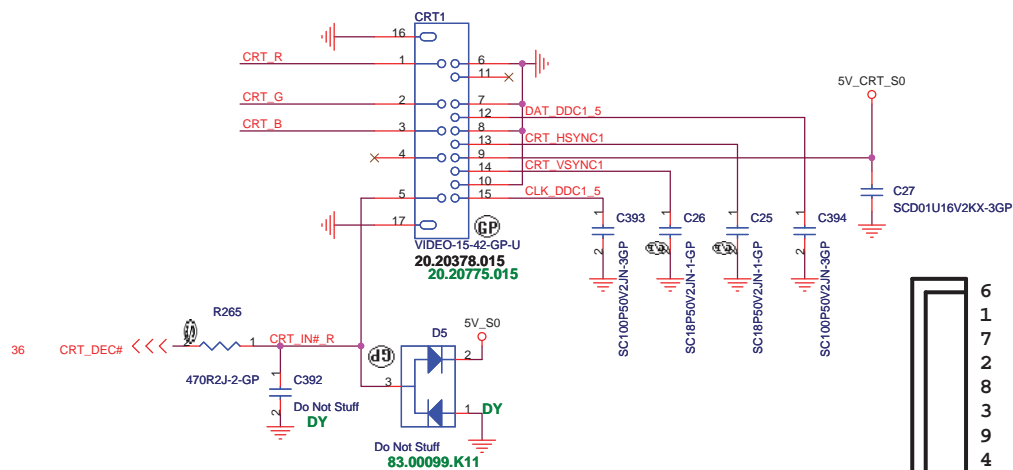


Layout Note:

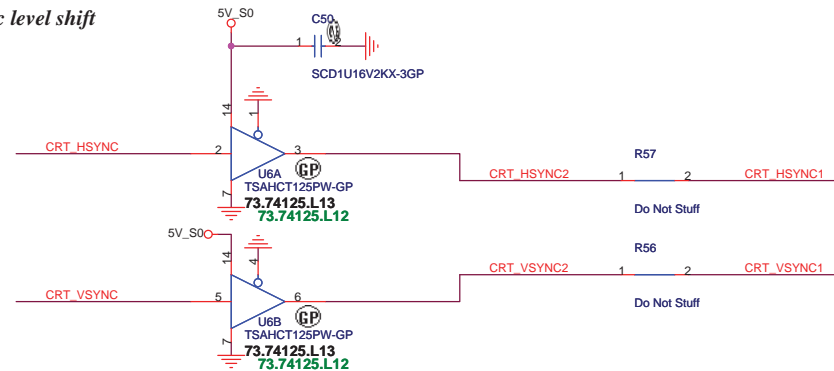
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



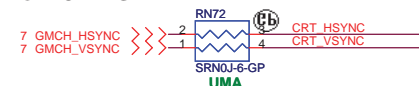
CRT I/F & CONNECTOR



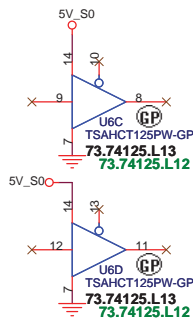
Hsync & Vsync level shift



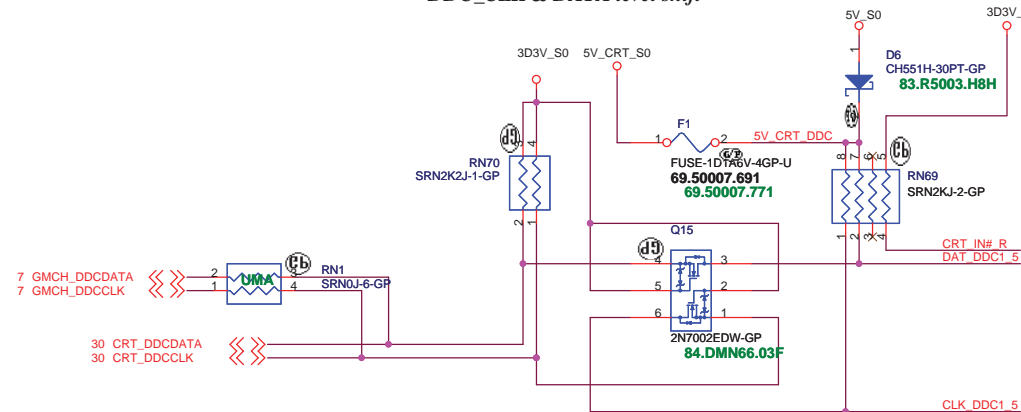
For UMA CRT



For DIS CRT

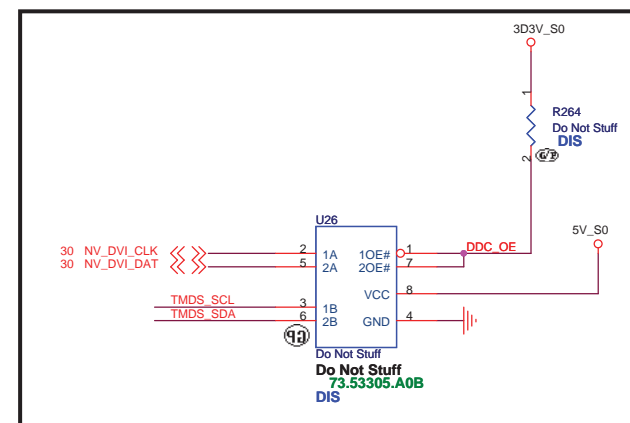


DDC_CLK & DATA level shift

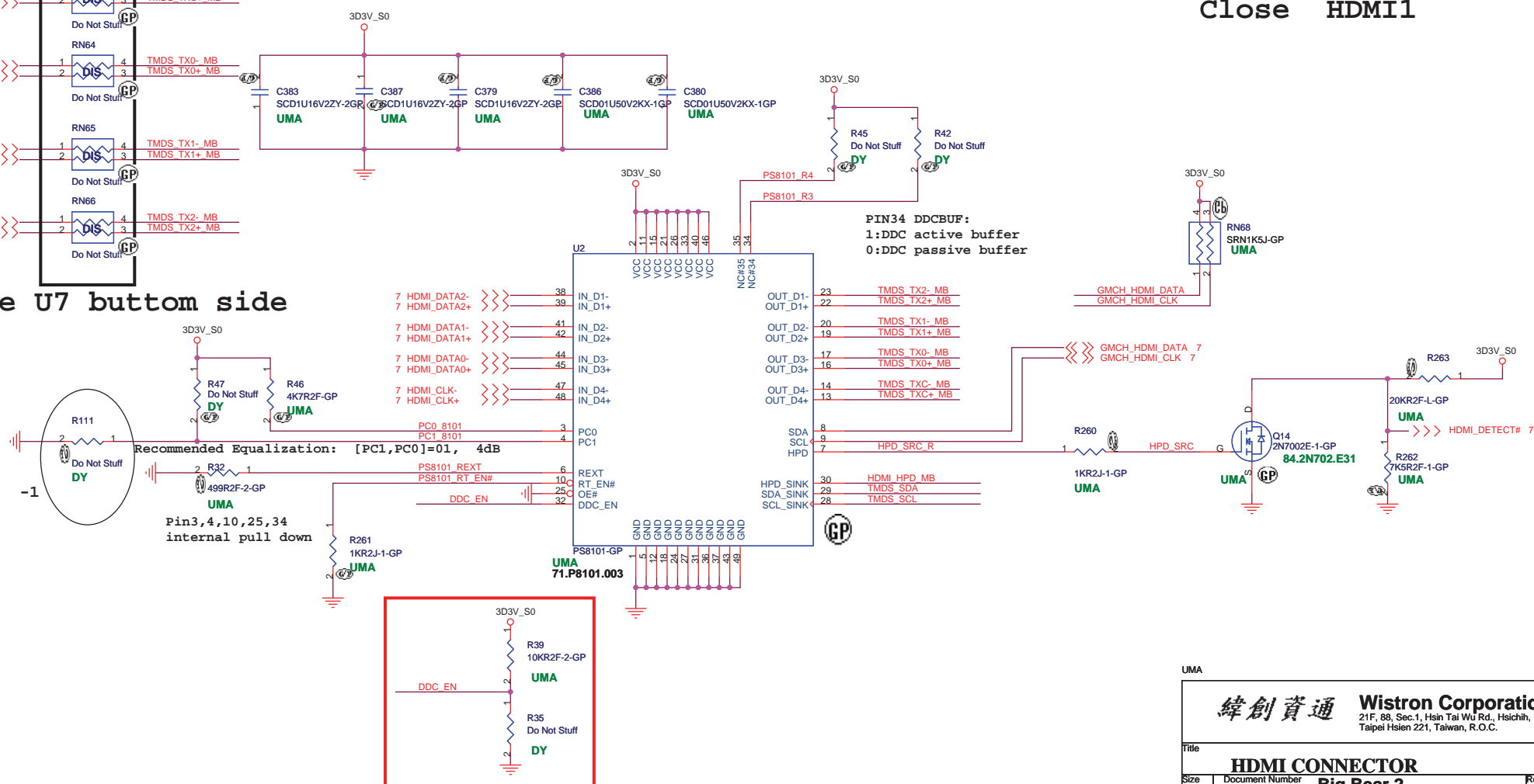


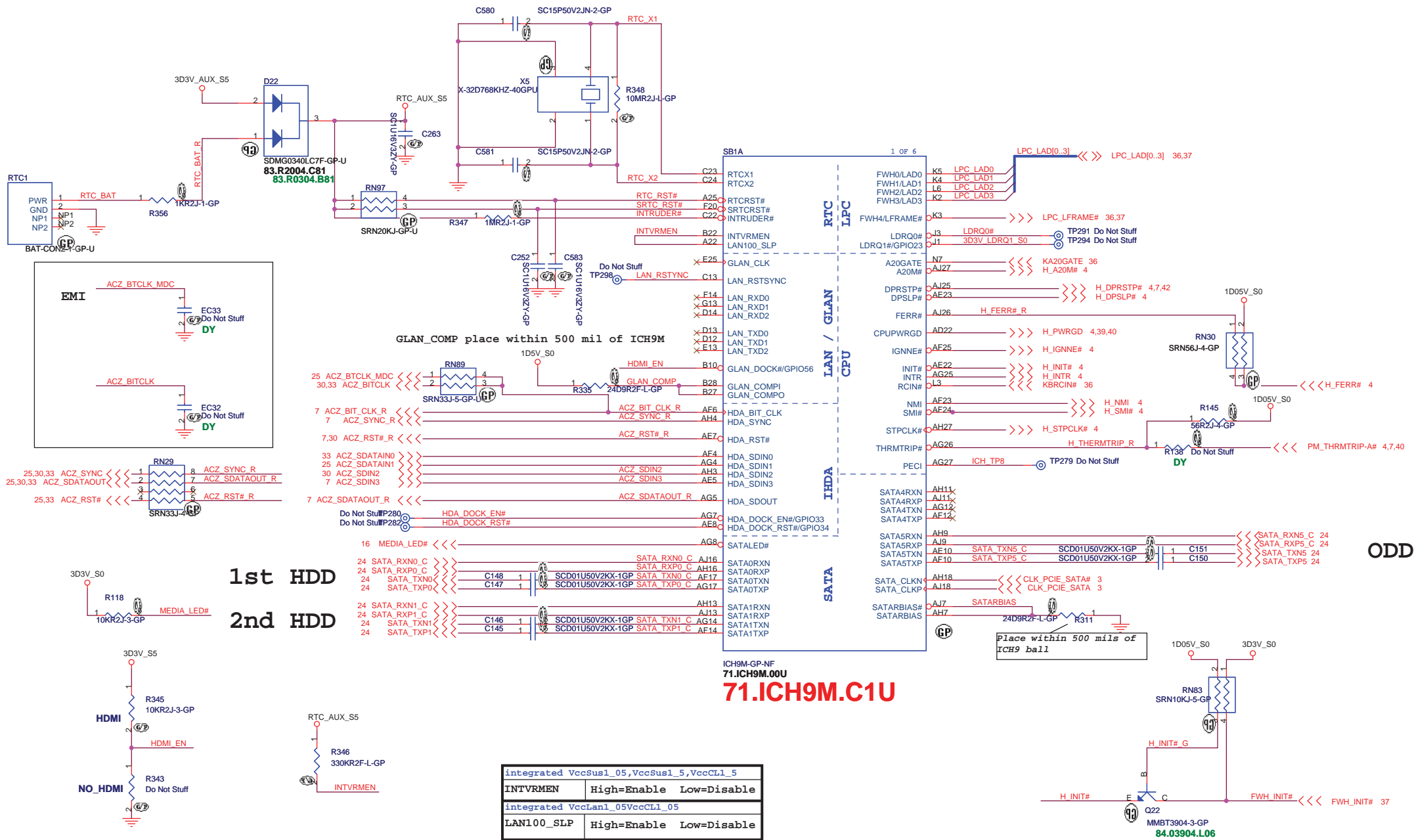
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Taipei Hsien 221, Taiwan, R.O.C.

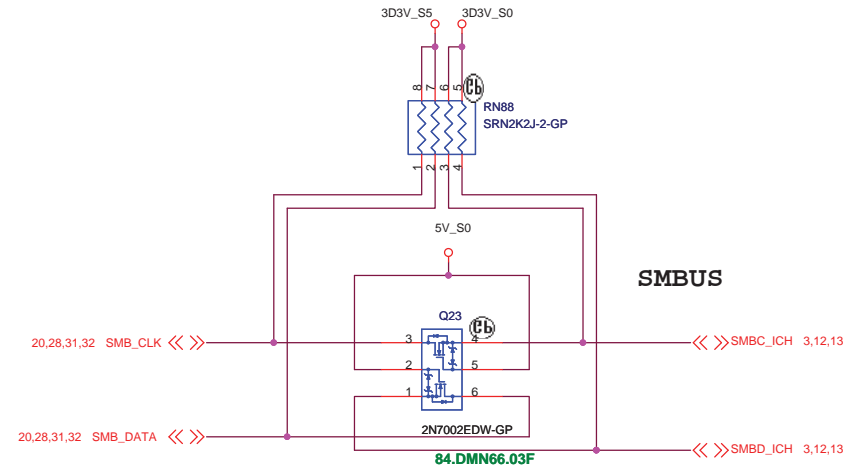
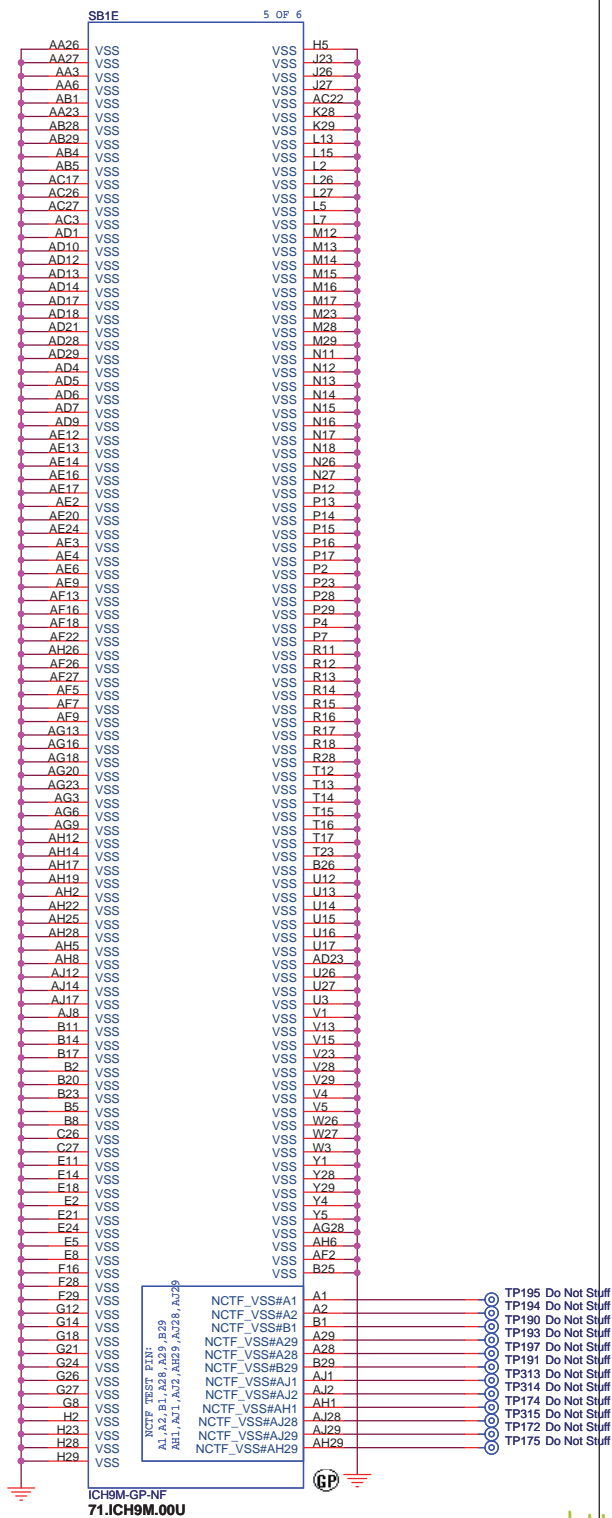


place U7 buttom side





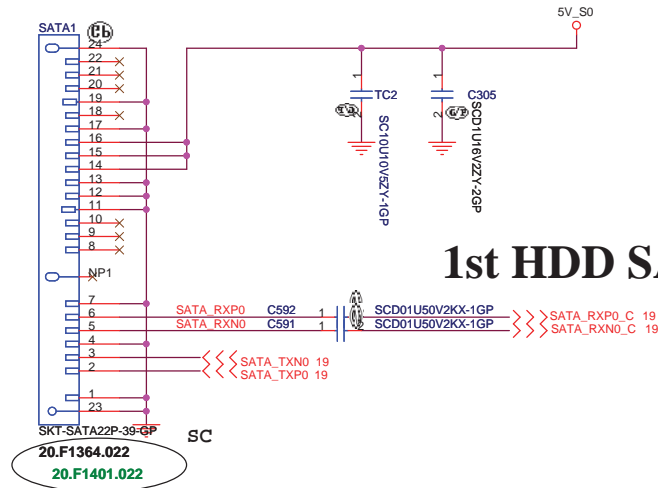




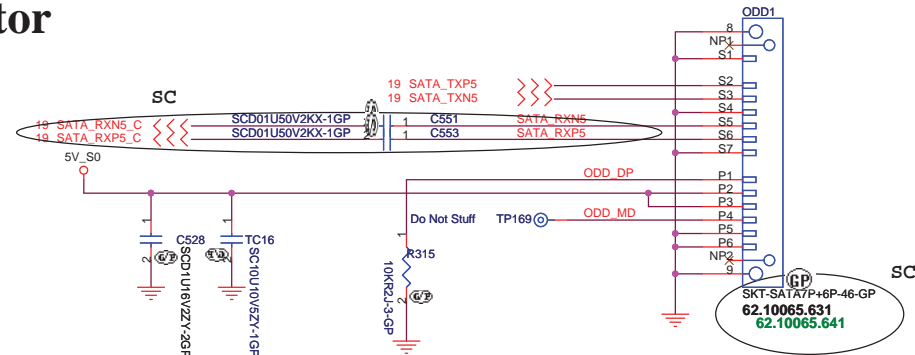
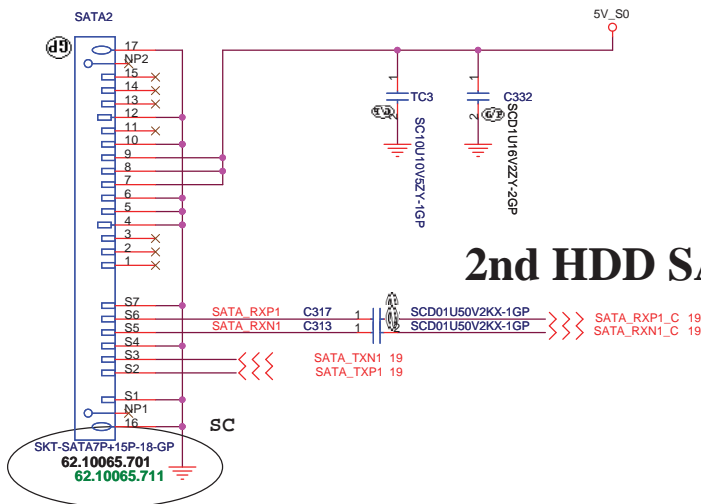


SATA ODD Connector

1st HDD SATA Connector

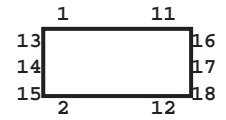
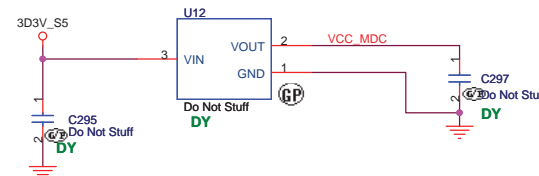
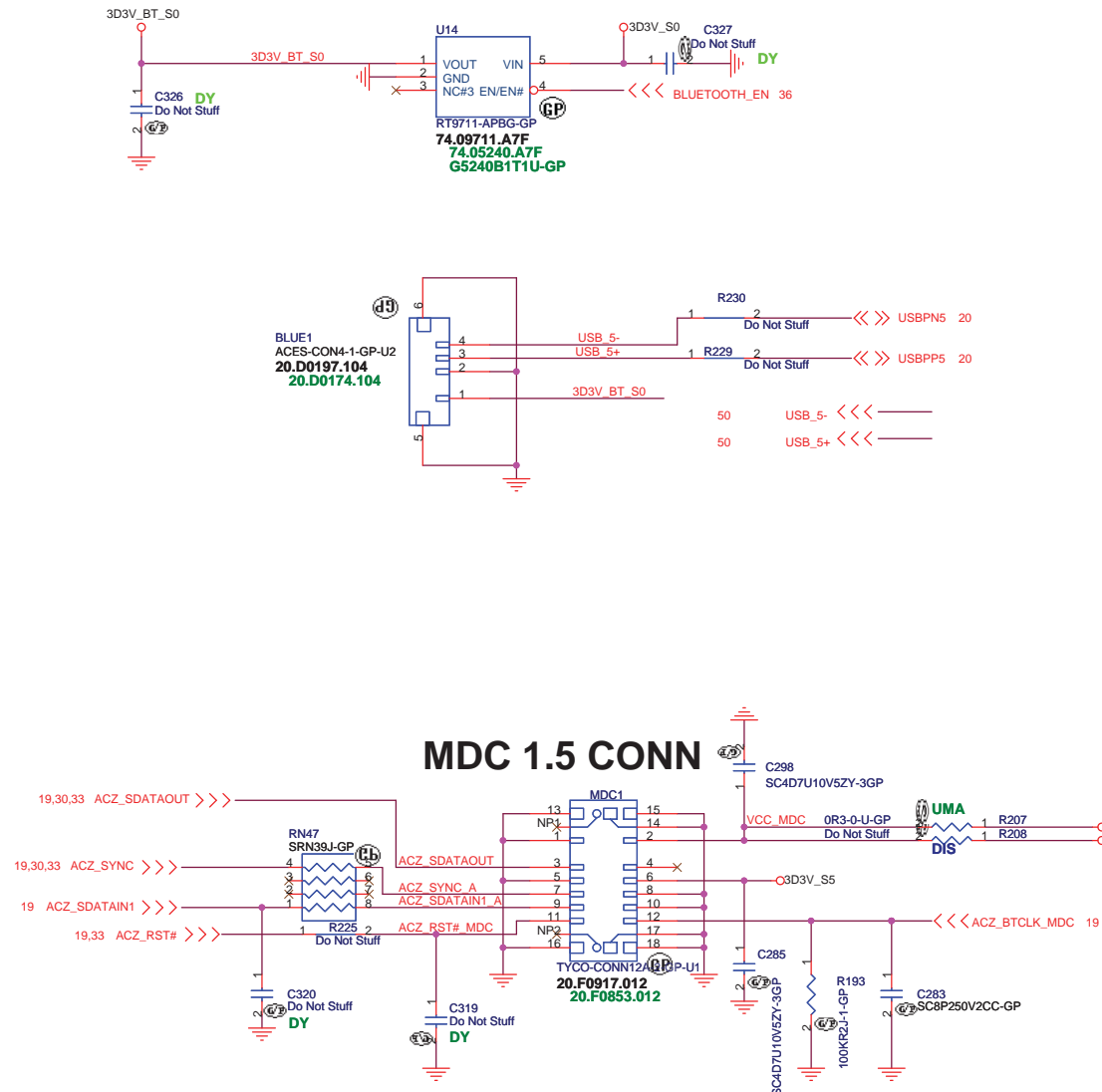


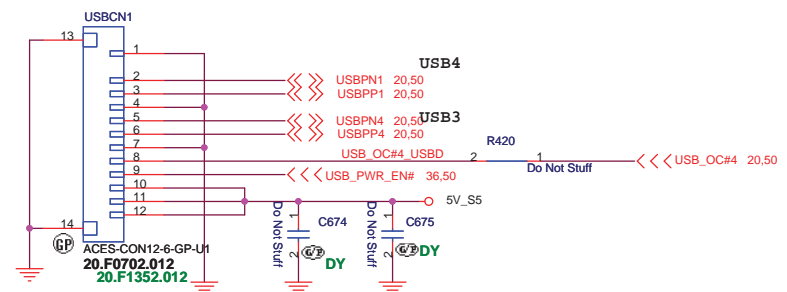
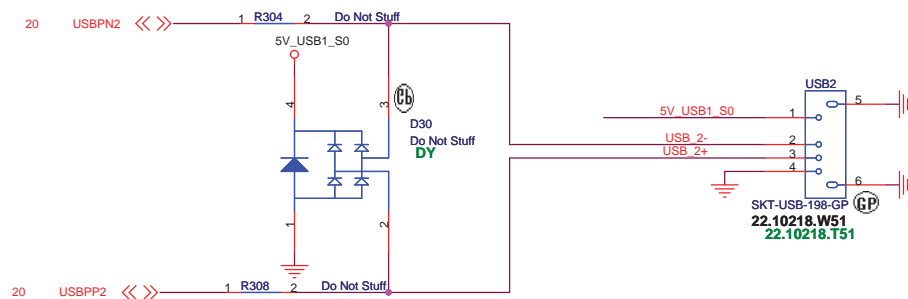
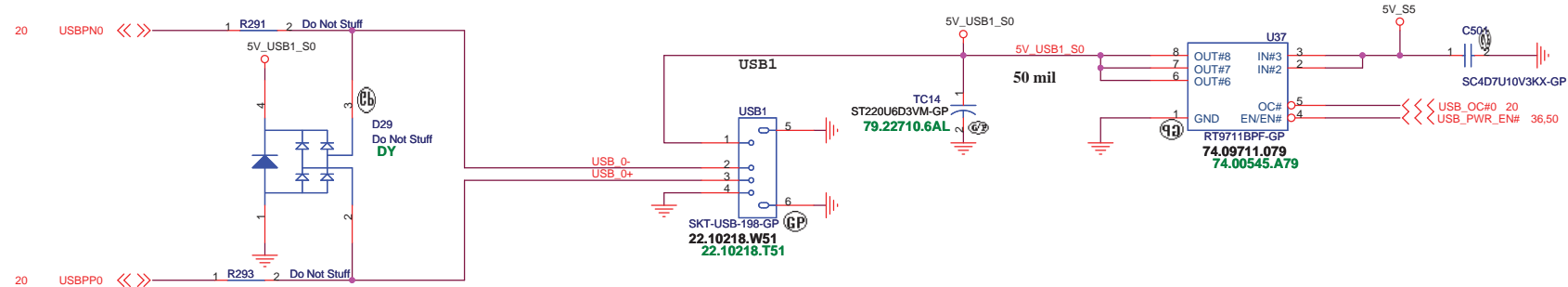
2nd HDD SATA Connector

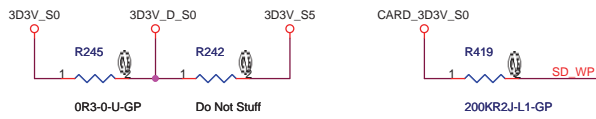


BLUETOOTH MODULE

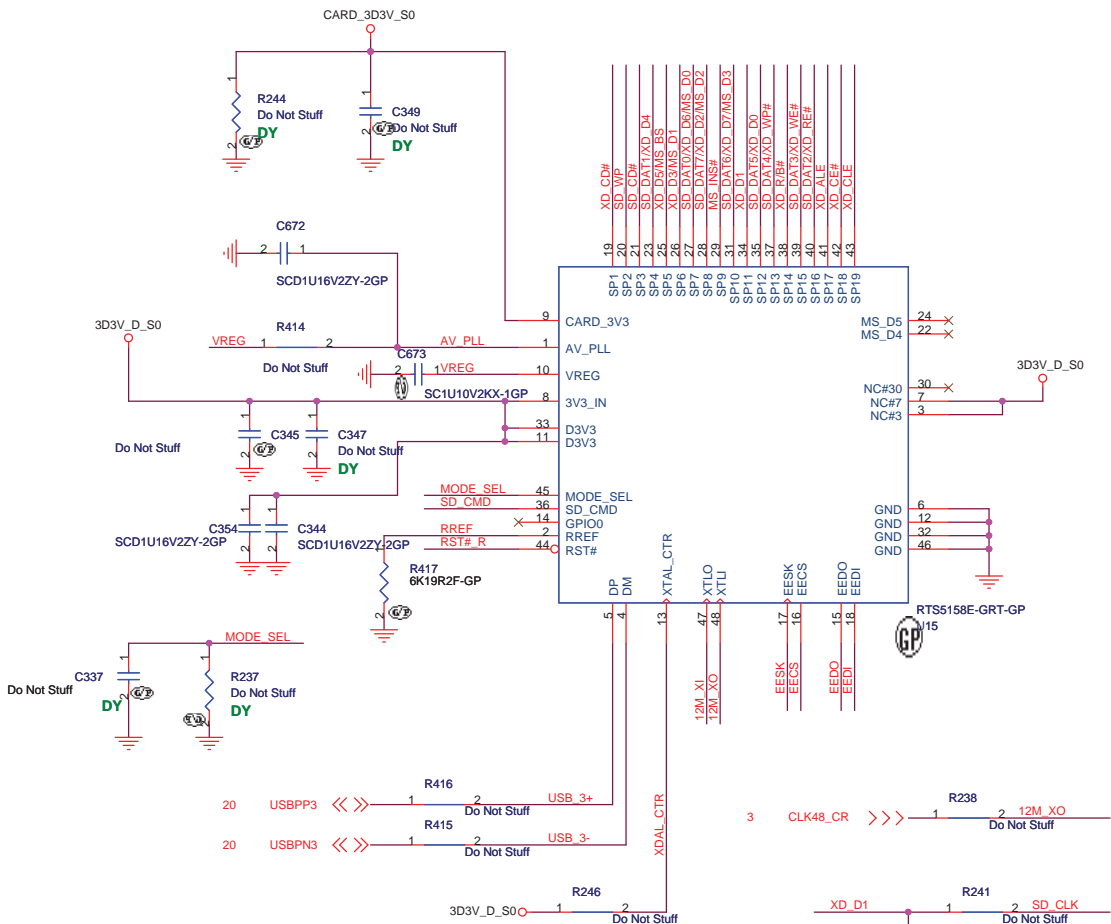
1.5A / High Active Voltage 2V



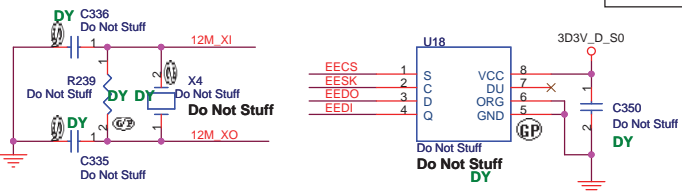
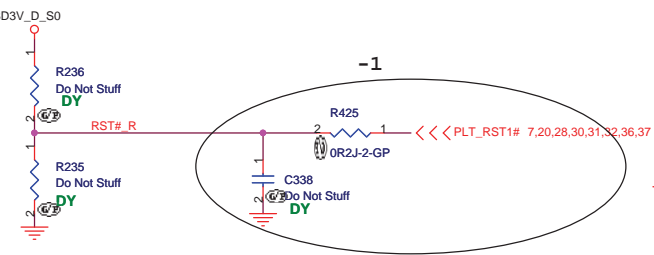
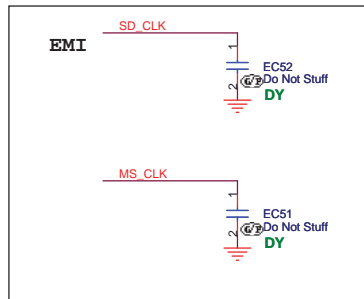
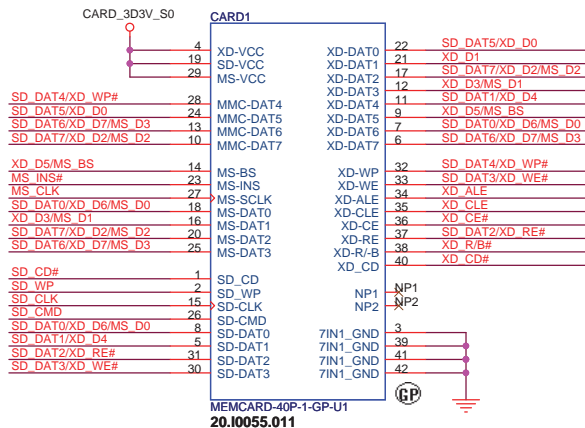
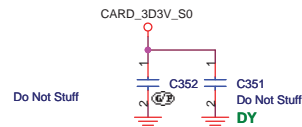




DY



7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

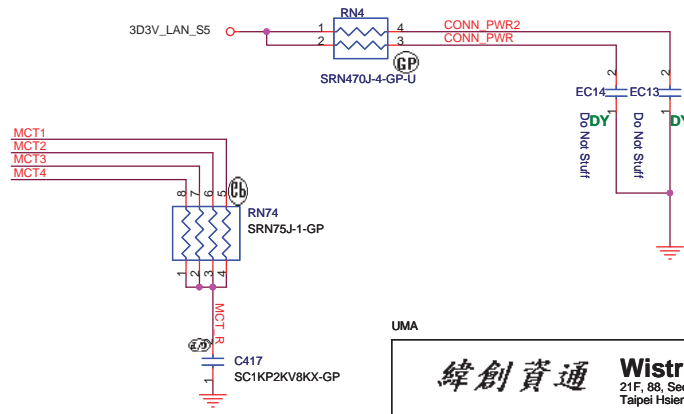
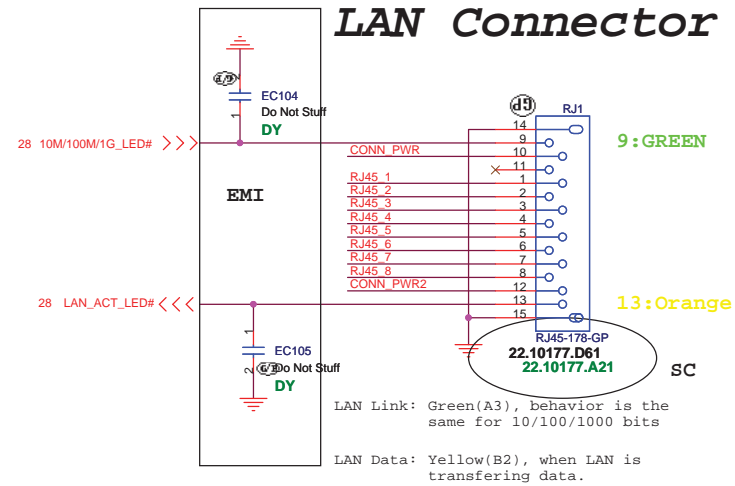
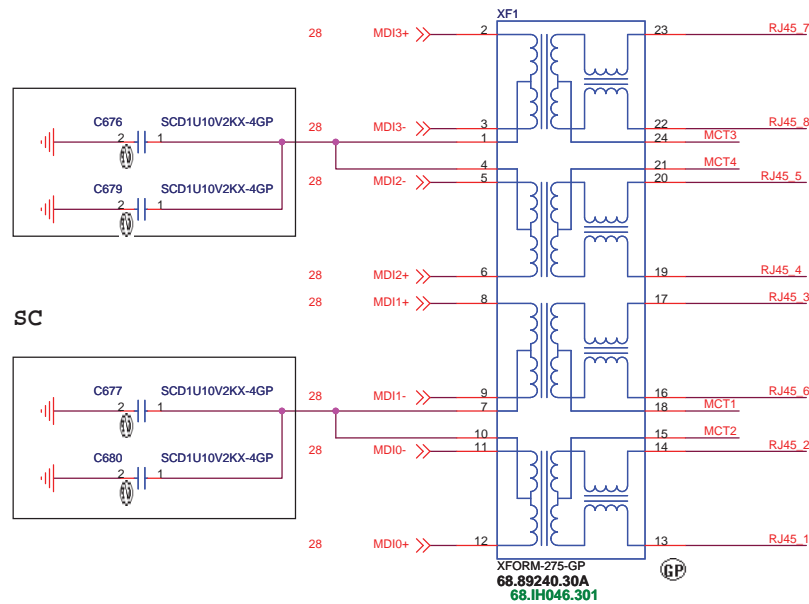


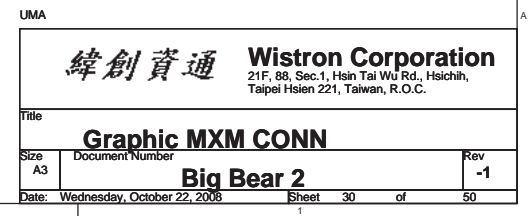
<http://hobi-elektronika.net>



LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

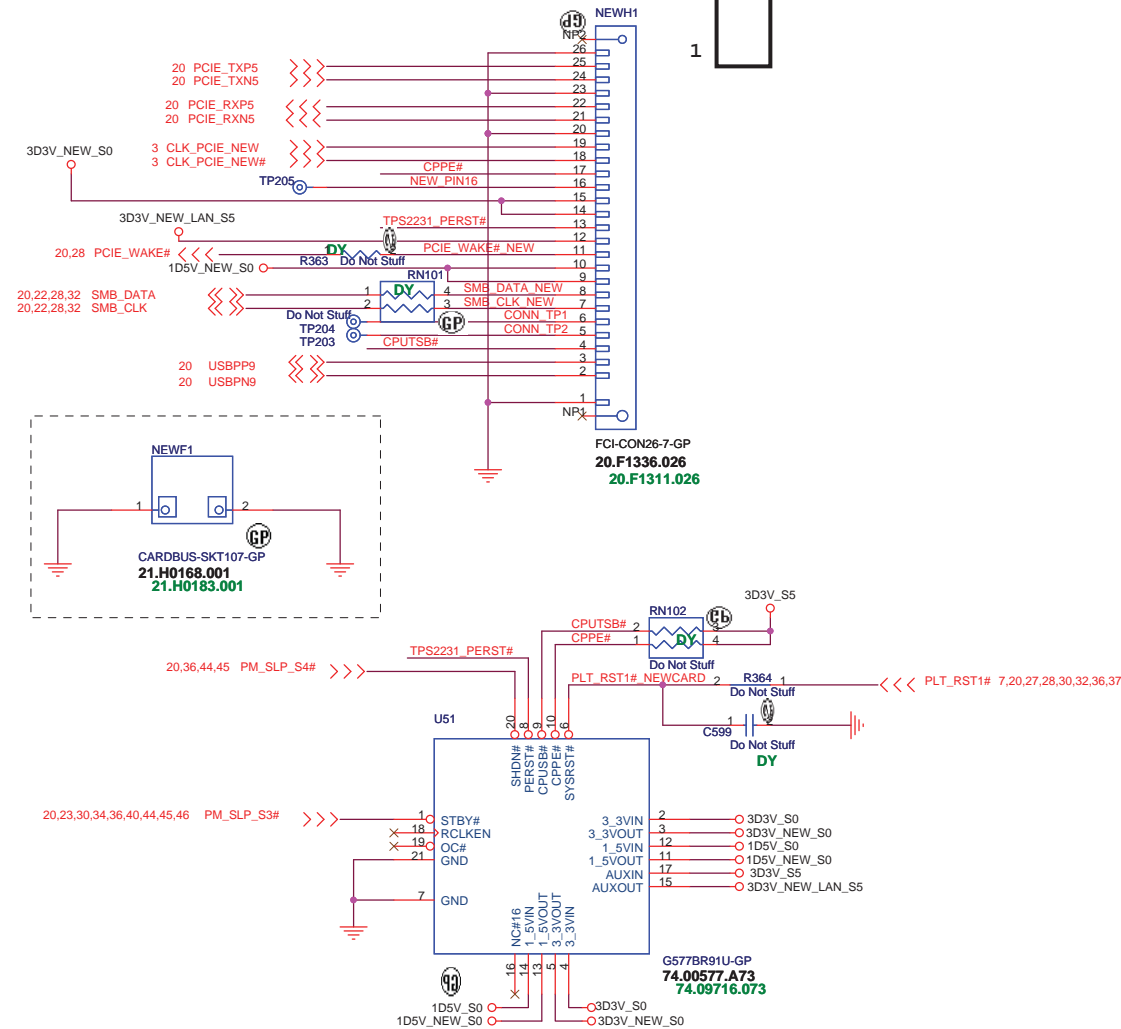




NEWCARD Connector

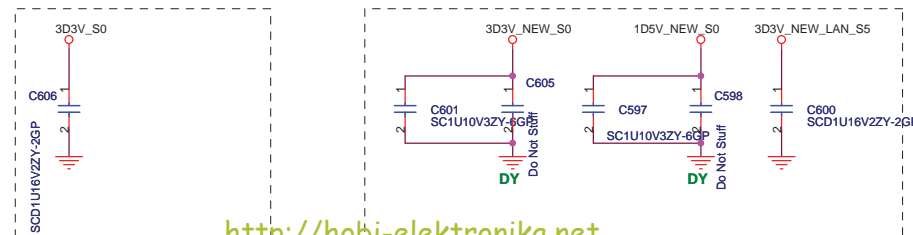
Reserve the symbol
for bottom side
connector

TOP VIEW



Place them Near to Chip

Place them Near to Connector



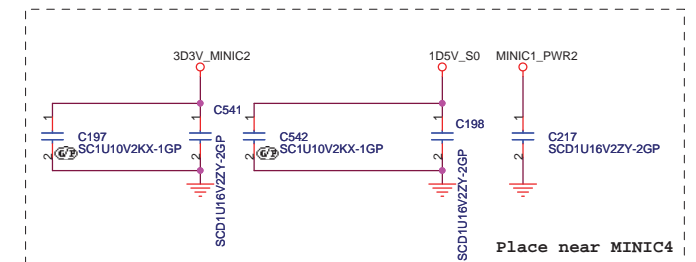
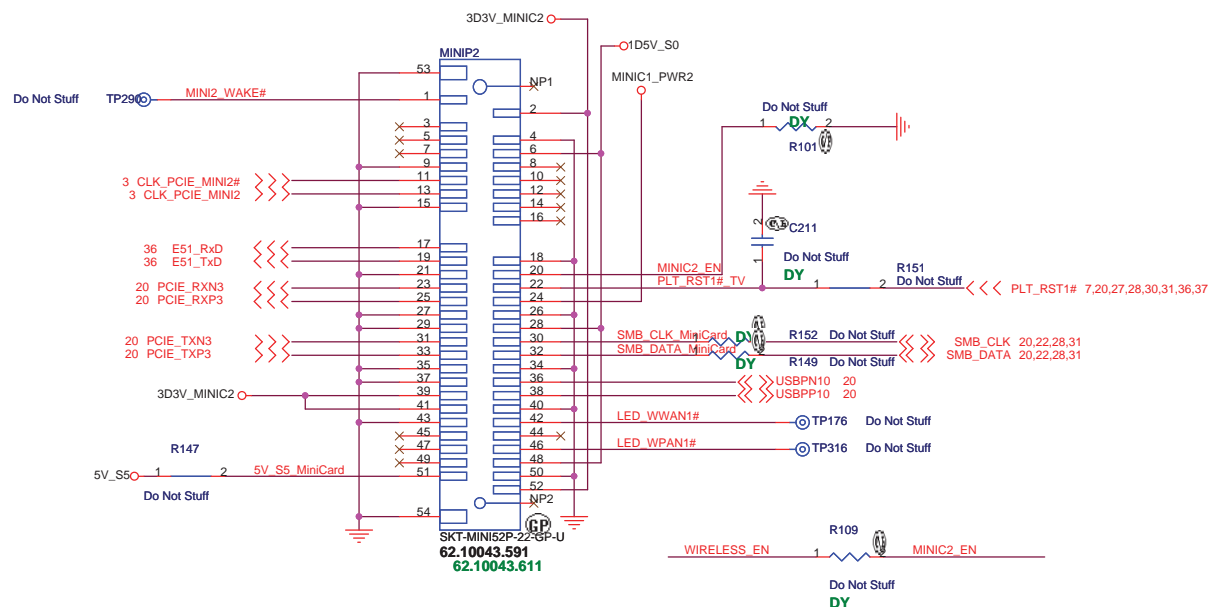
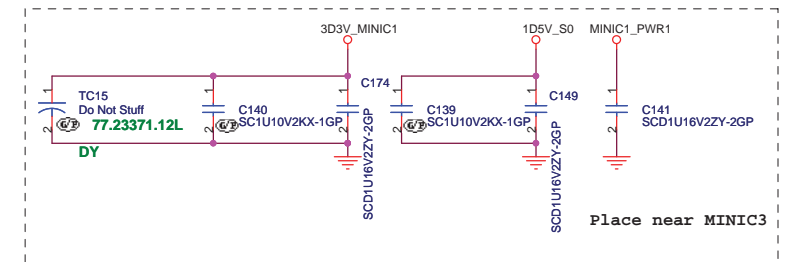
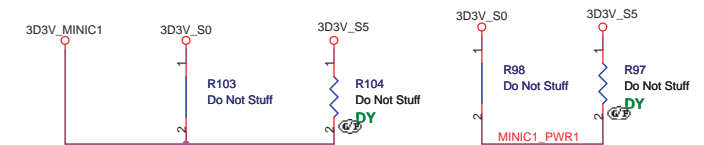
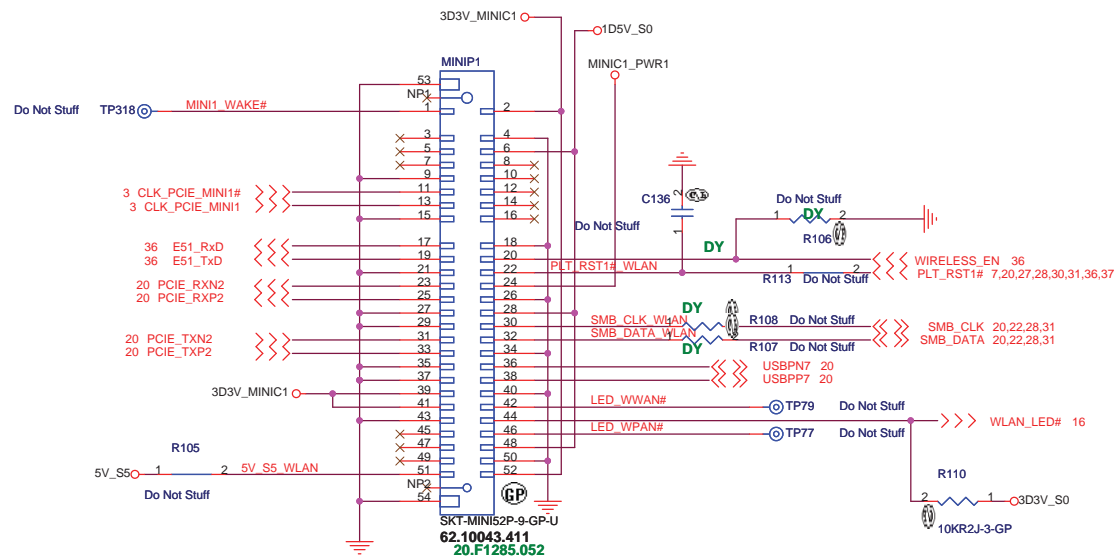
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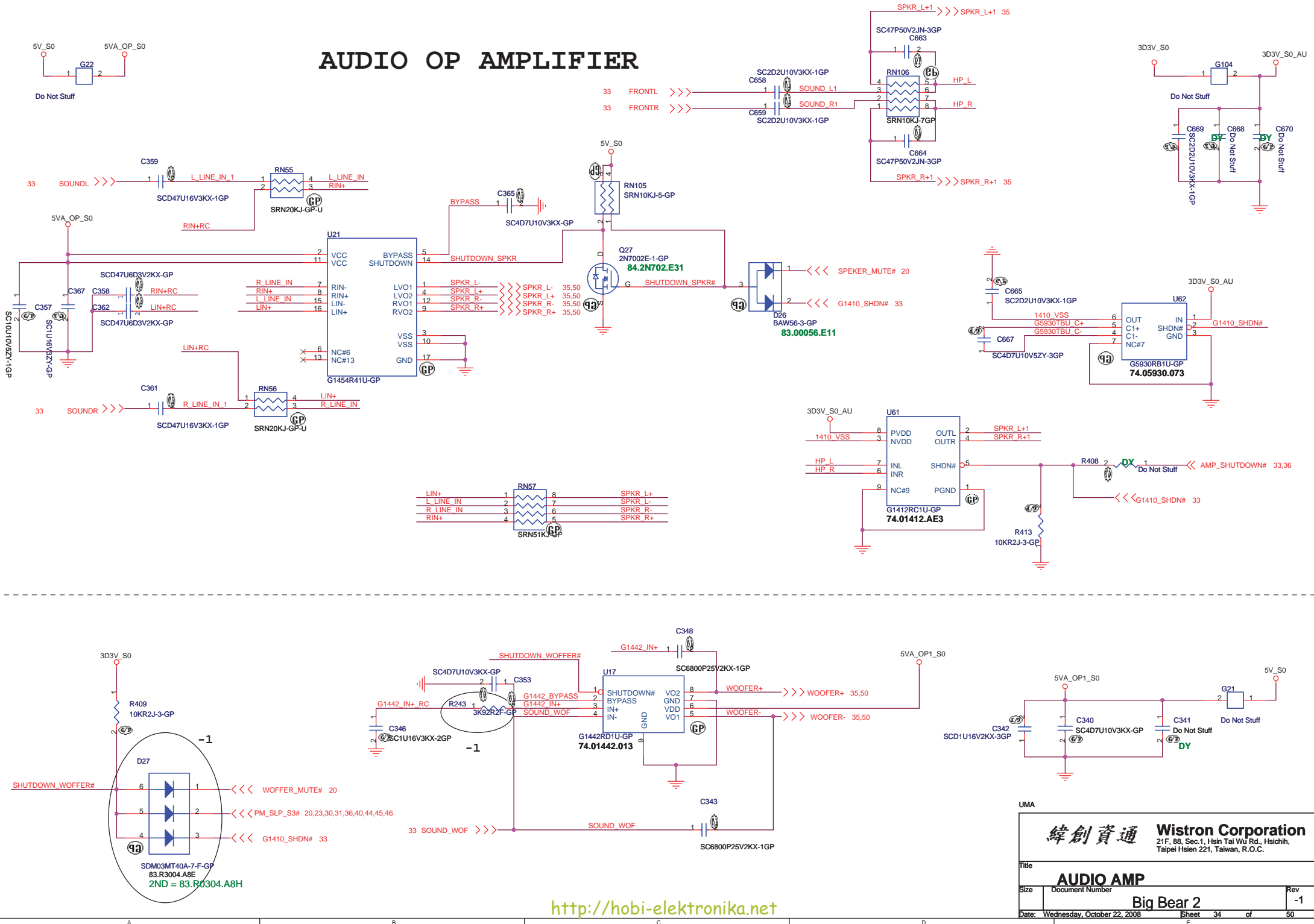
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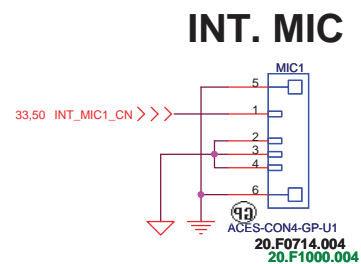
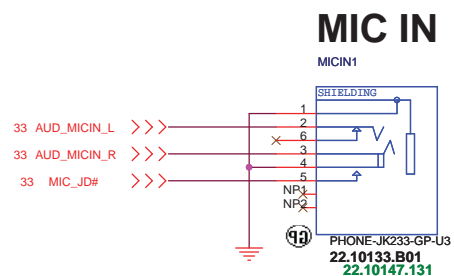
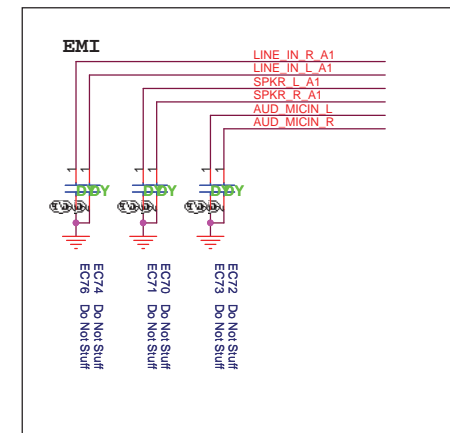
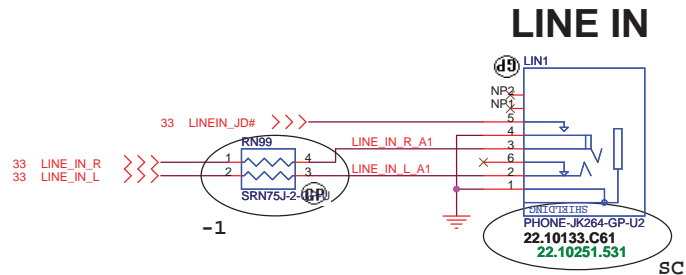
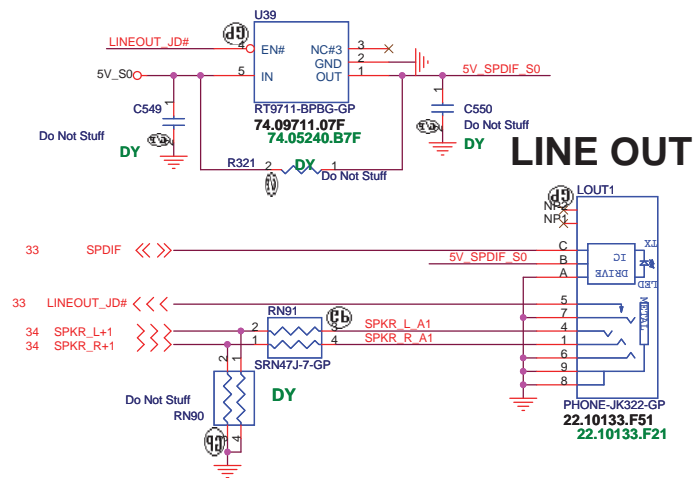
Title		NEW CARD	
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Mini Card Connector(WLAN)

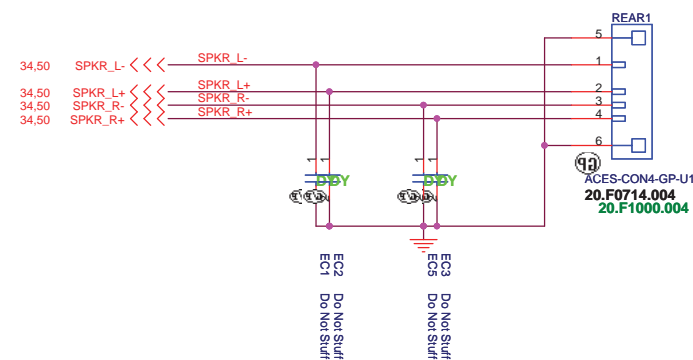


AUDIO OP AMPLIFIER

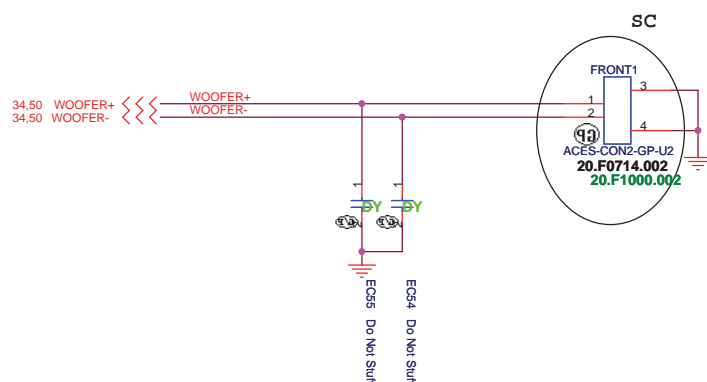




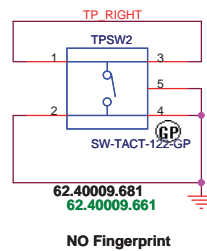
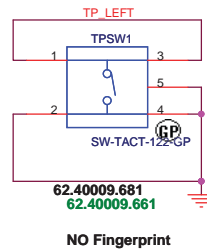
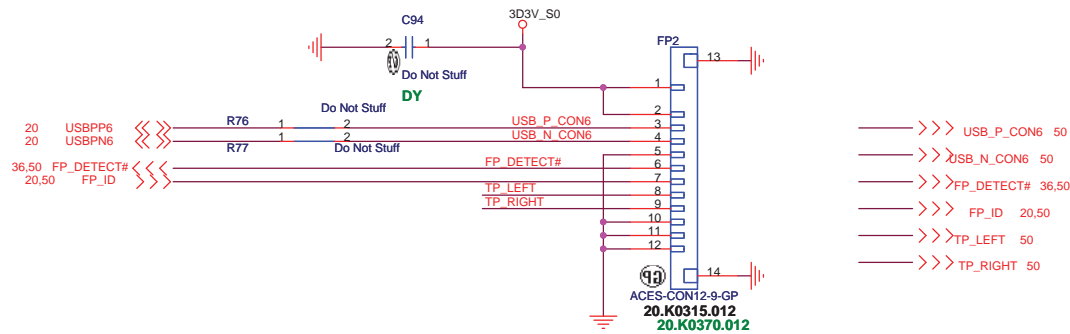
REAR Speaker



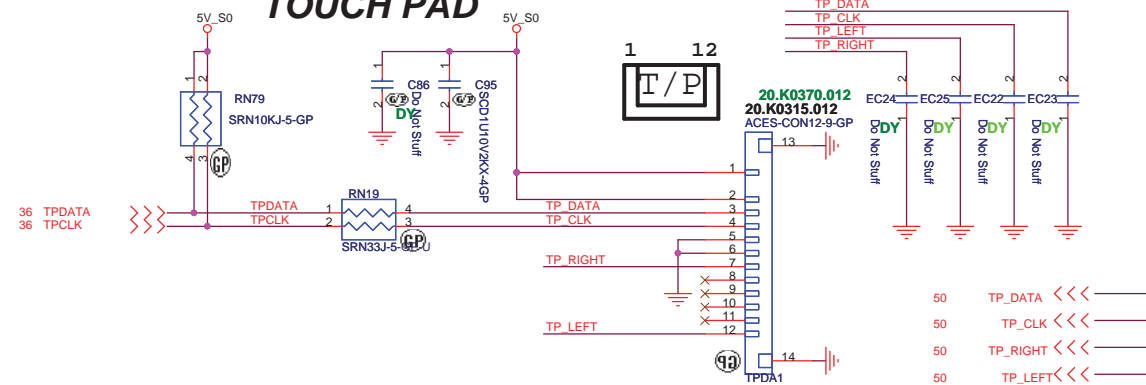
SUBWOOFER



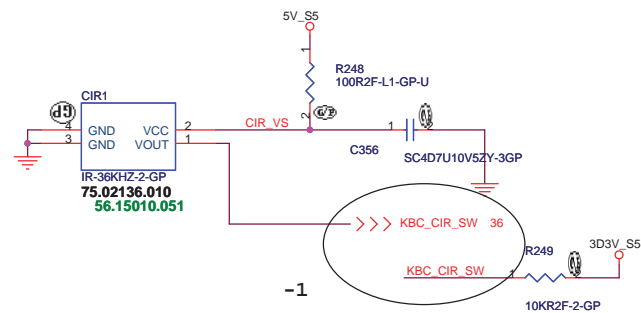
Finger printer



TOUCH PAD



CIR Module

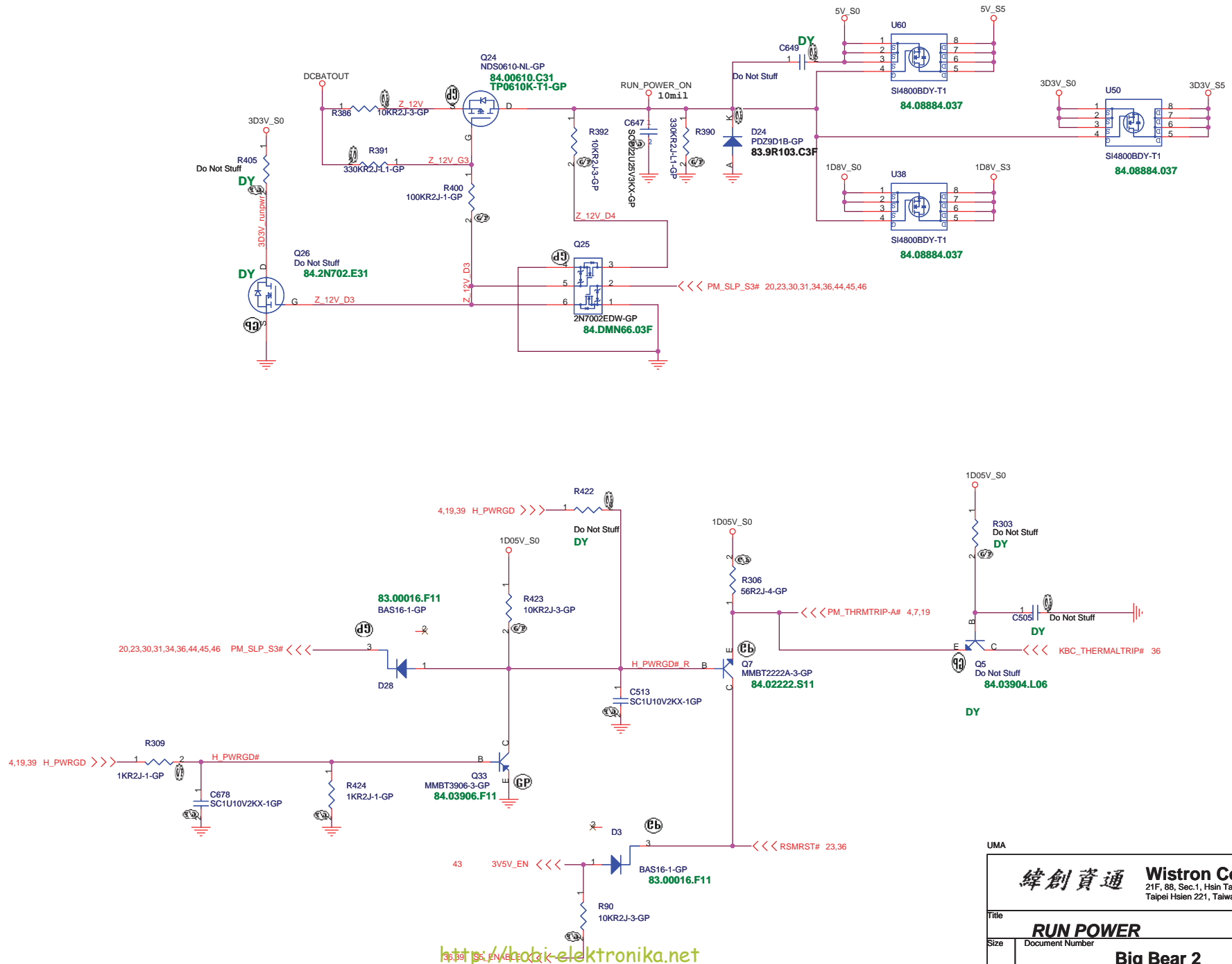


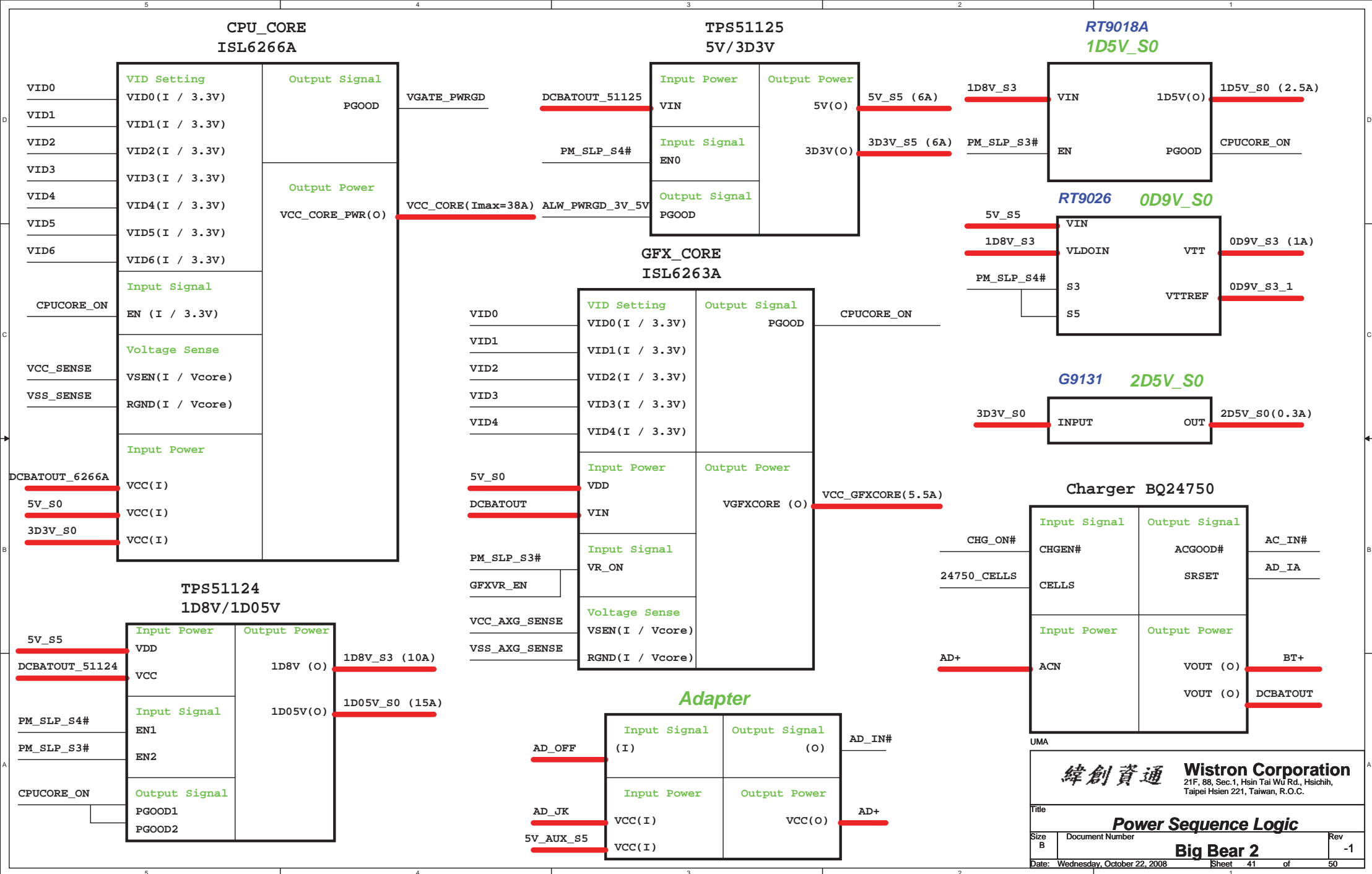
Check test point

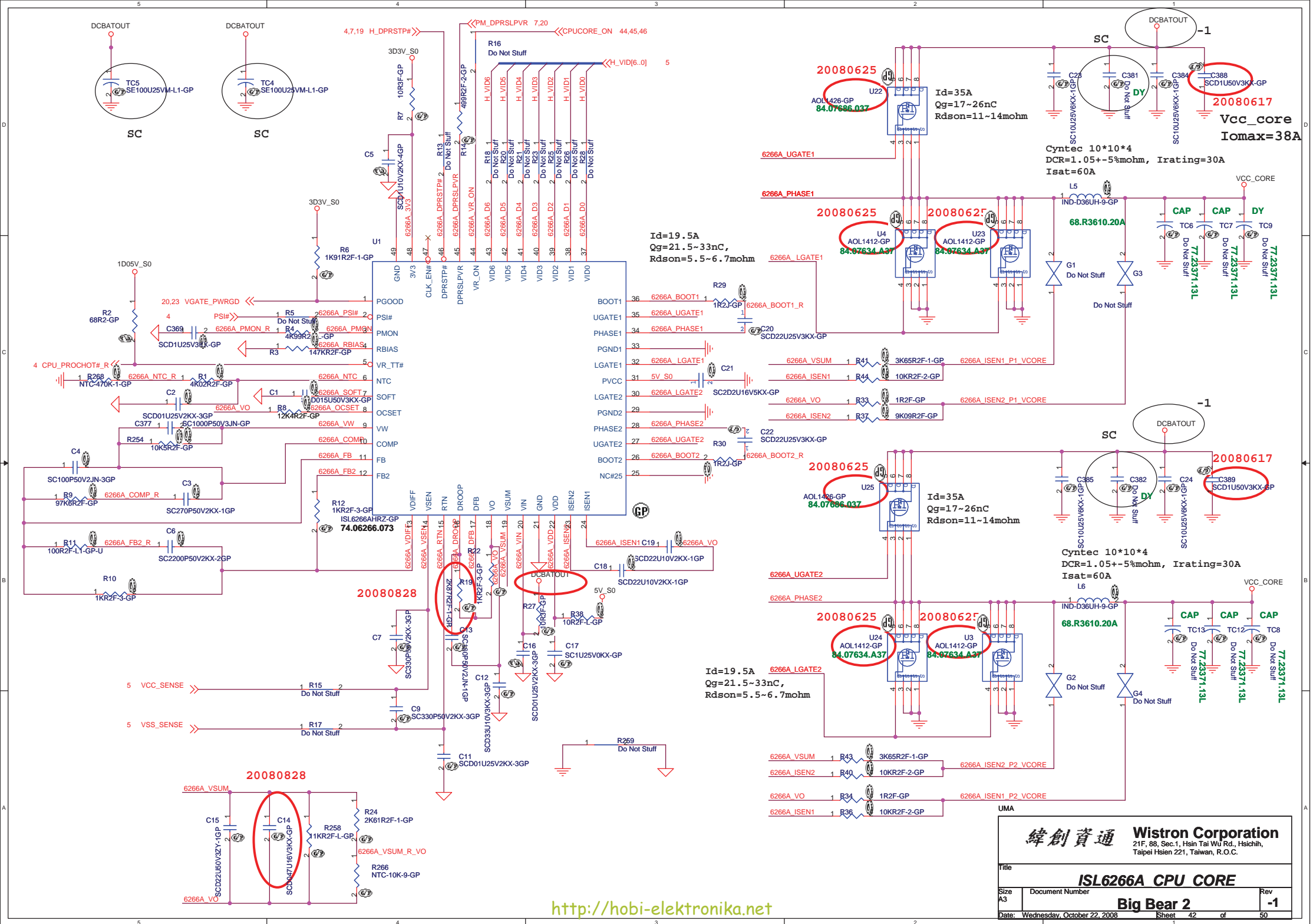
- 3D3V_S0 — TP202 Do Not Stuff
- 3D3V_AUX_S5 — TP141 Do Not Stuff
- 3D3V_S5 — TP120 Do Not Stuff
- 5V_S5 — TP130 Do Not Stuff
- 20,36 PM_PWRBTN# <<< — TP115 Do Not Stuff
- 4,19,40 H_PWRGD <<< — TP320 Do Not Stuff
- 36,40 S5_ENABLE <<< — TP110 Do Not Stuff
- 4,6 H_CPURST# <<< — TP278 Do Not Stuff

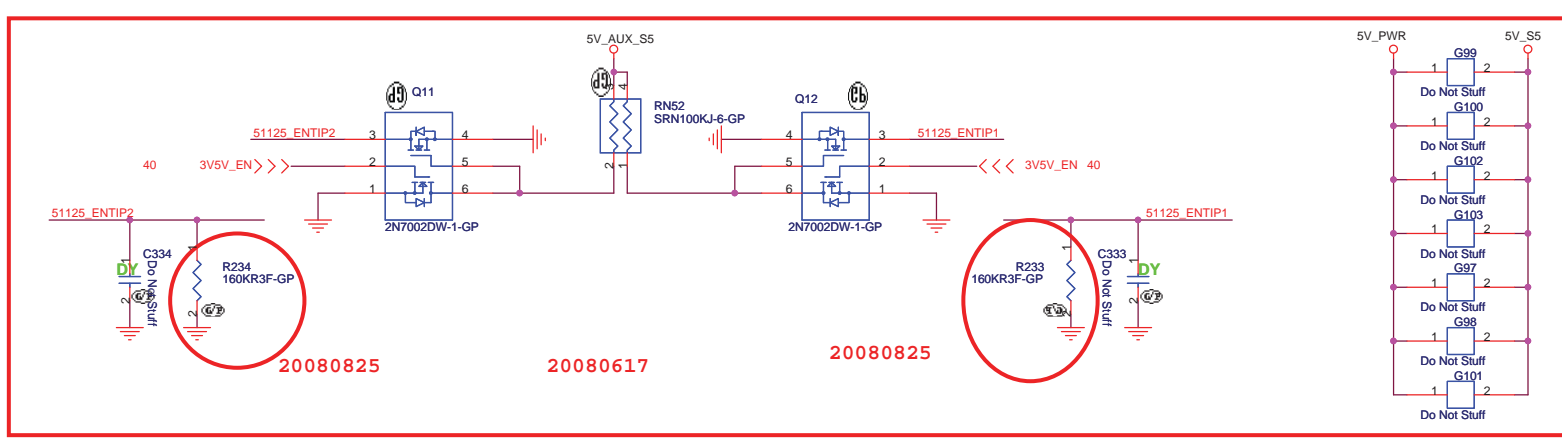
Test Point 放在Dimm Door 打開可量測處

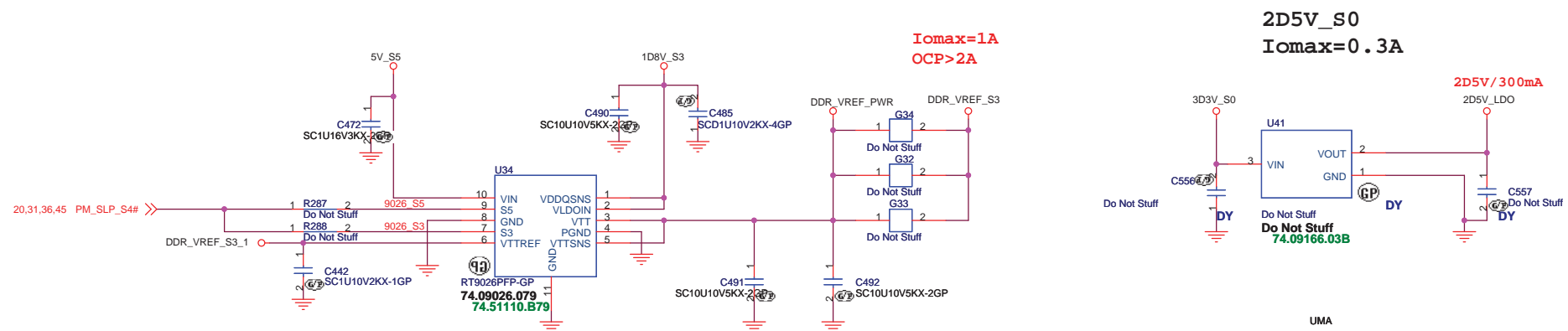
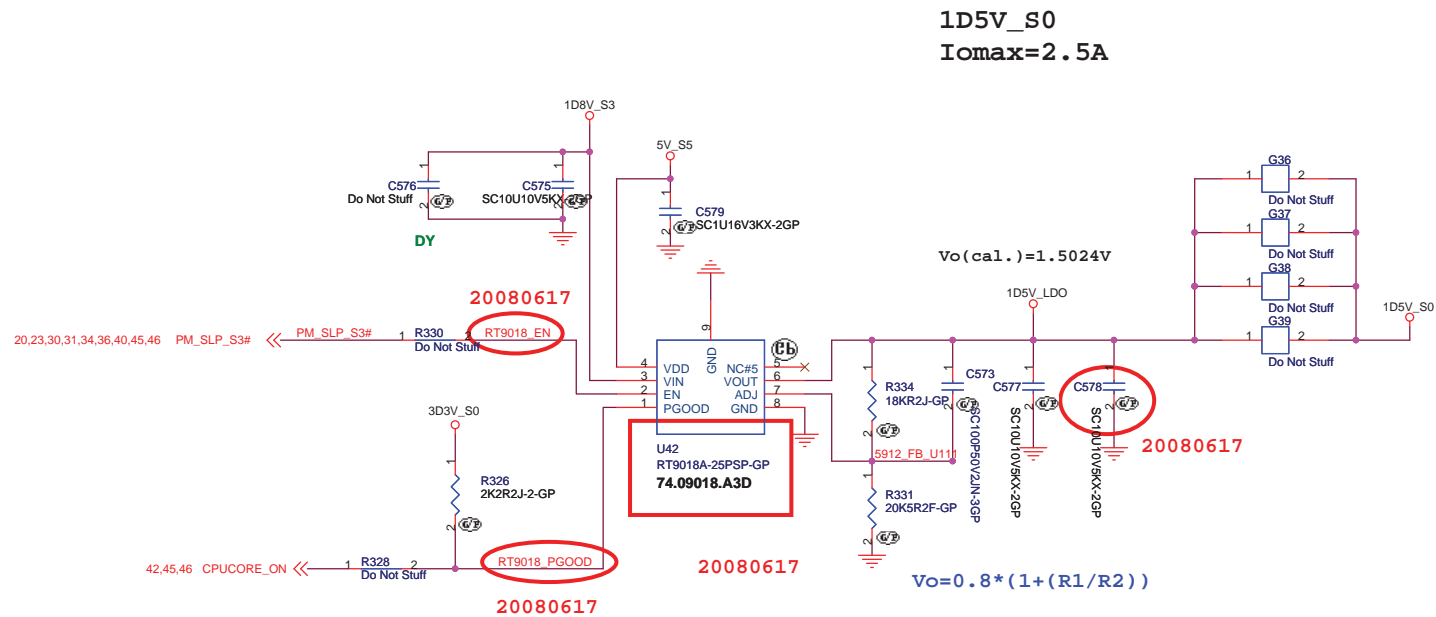
Run Power







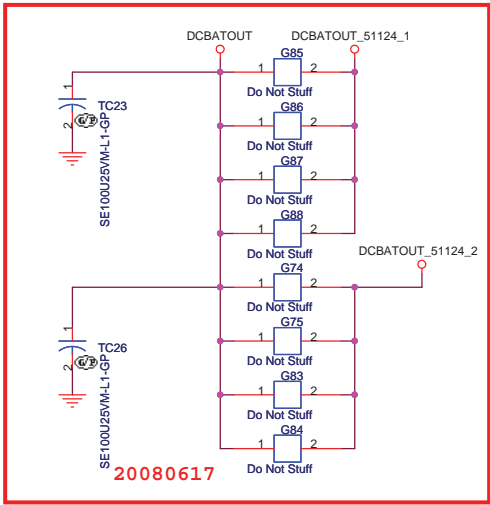




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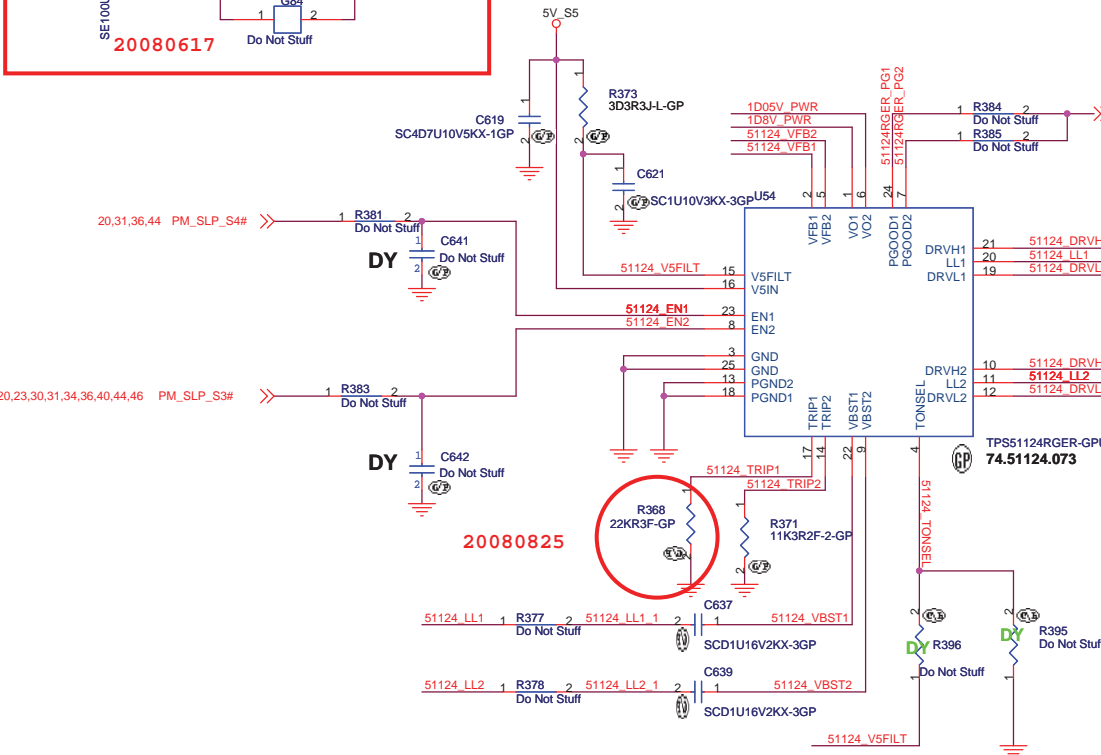
Title 1D5V & 0D9V & 2D5V		
Size A3	Document Number Big Bear 2	Rev -1
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$$V_{trip}(mV) = R_{trip}(Kohm) * I_{0}(uA)$$

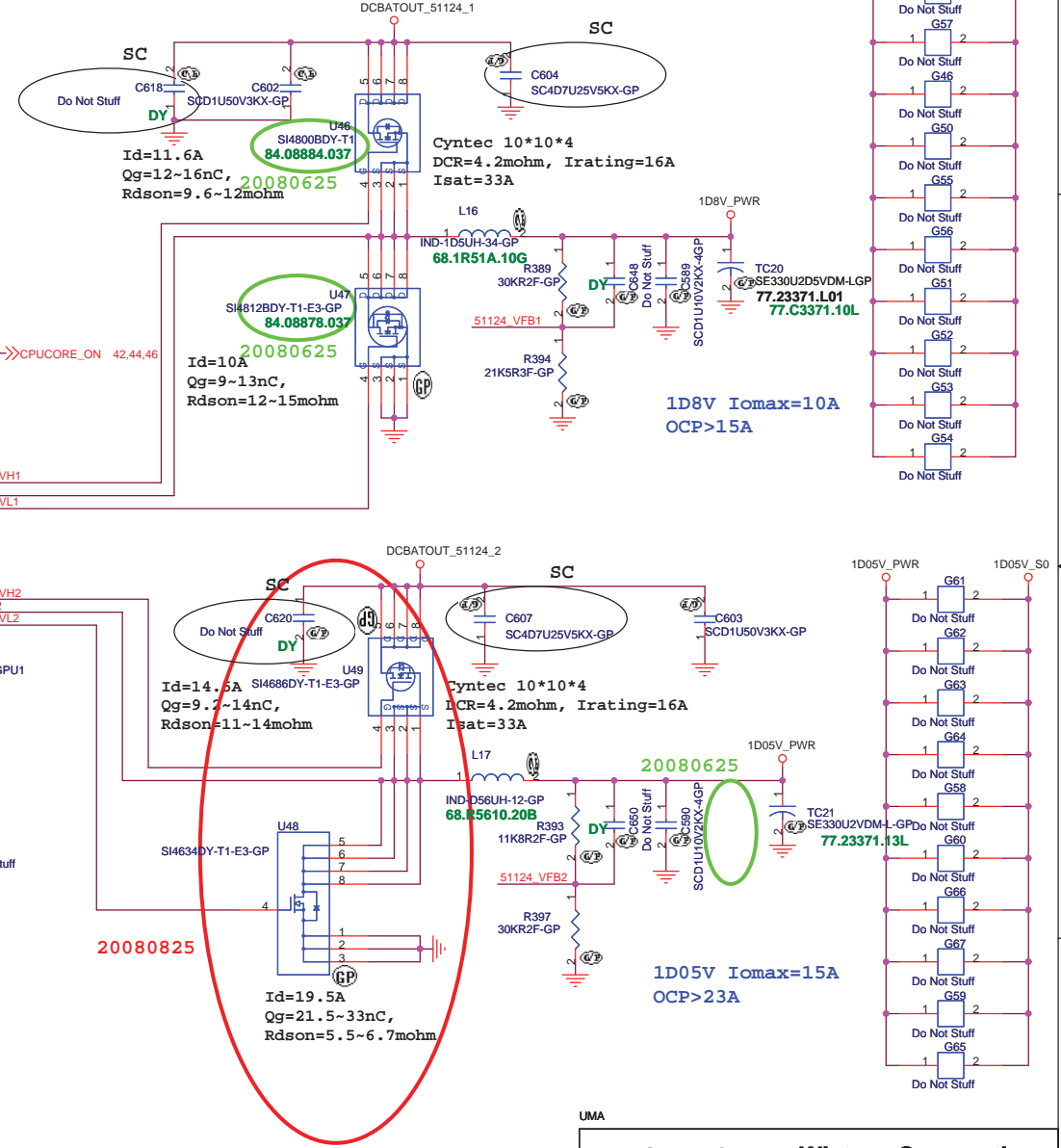
$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

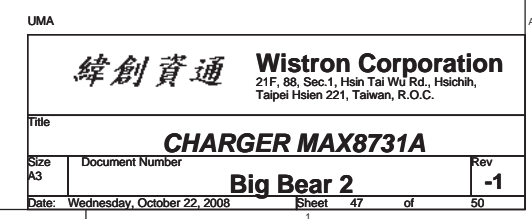
$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode



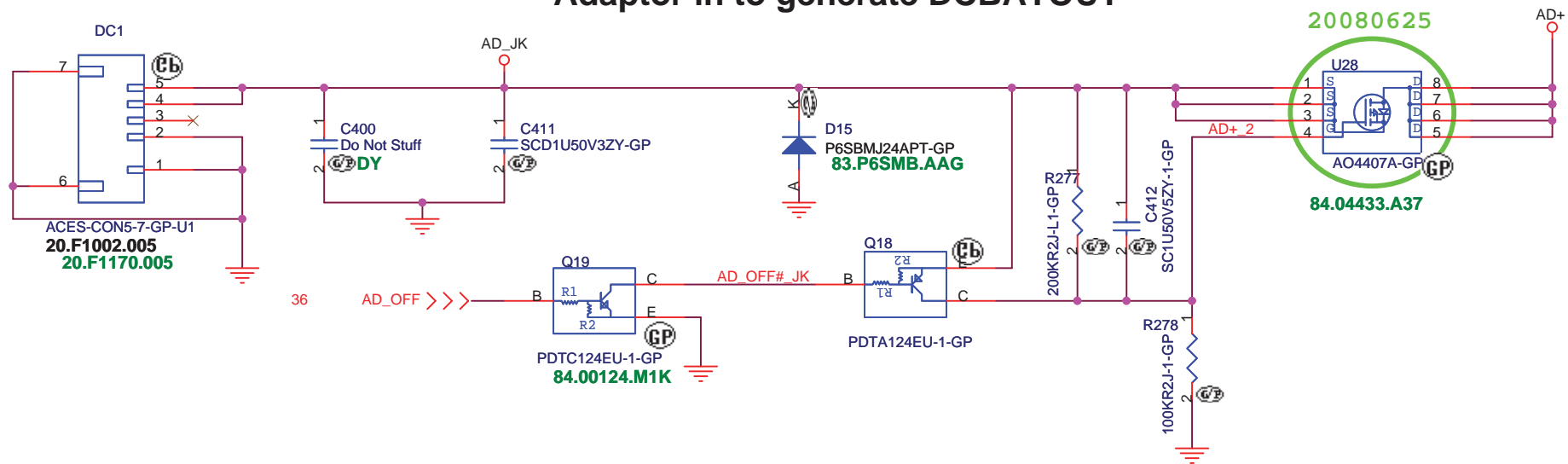
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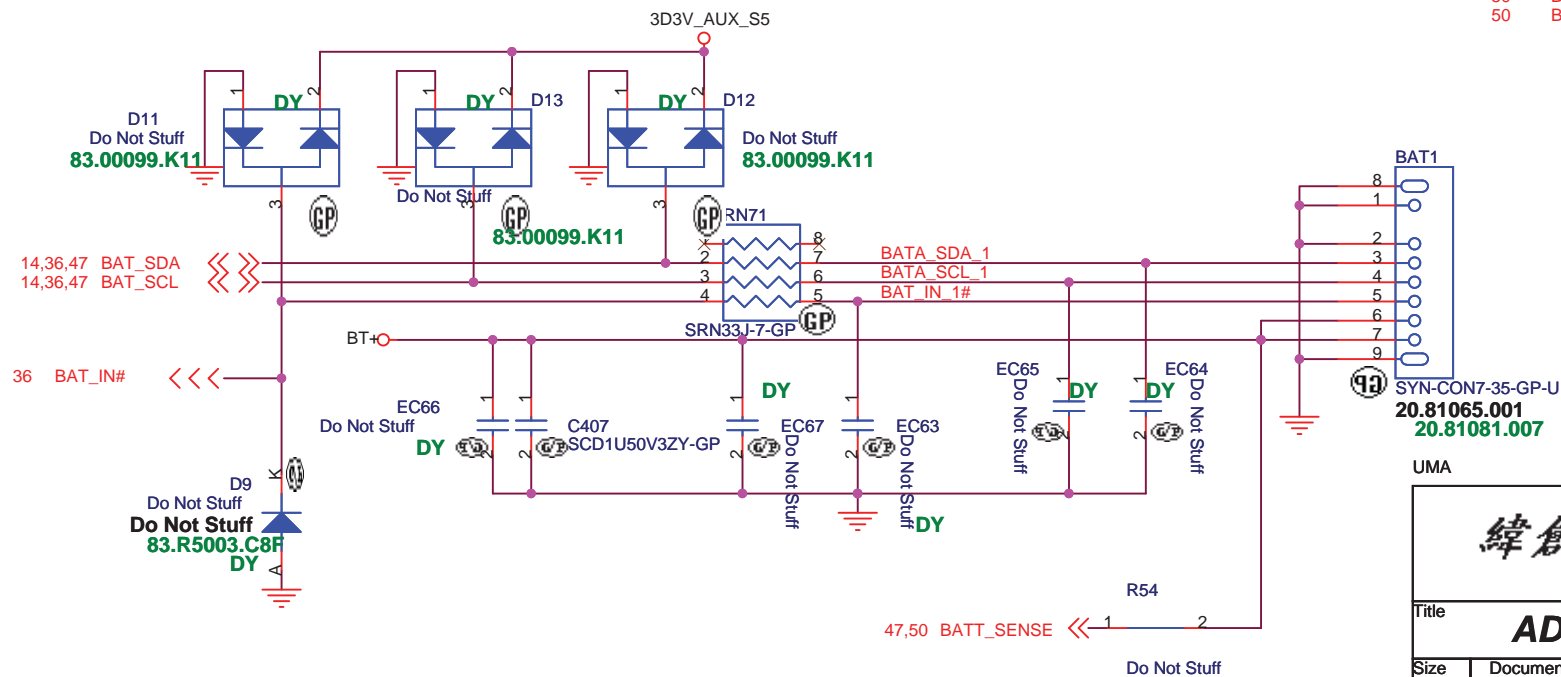
TPS51124 1D8V 1D05V			
Size A3	Document Number	Rev	-1
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



47,50 BATT_SENSE <<< BATT_SENSE

50 BAT_IN_1# <<< BAT_IN_1#

50 BATA_SDA_1 <<< BATA_SDA_1

50 BATA_SCL_1 <<< BATA_SCL_1

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Title AD/BATT CONN

Size Document Number Rev -1

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STAND OFF

SPRING ON BOTTOM

CPU & NB

MDC

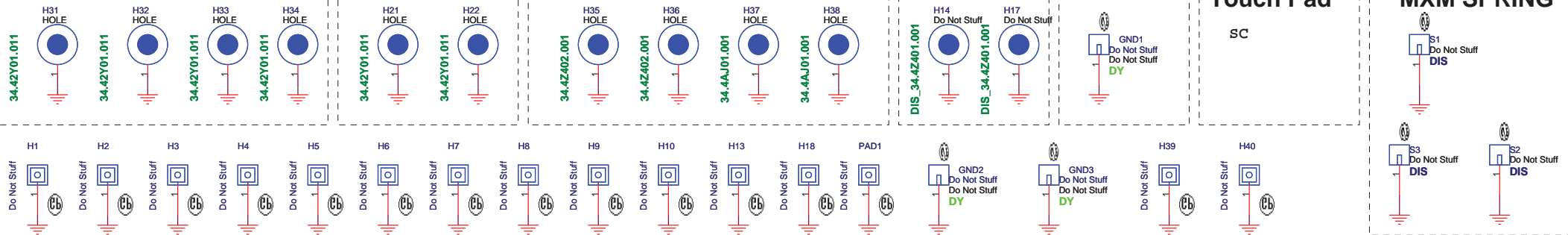
Mini Card

MXM

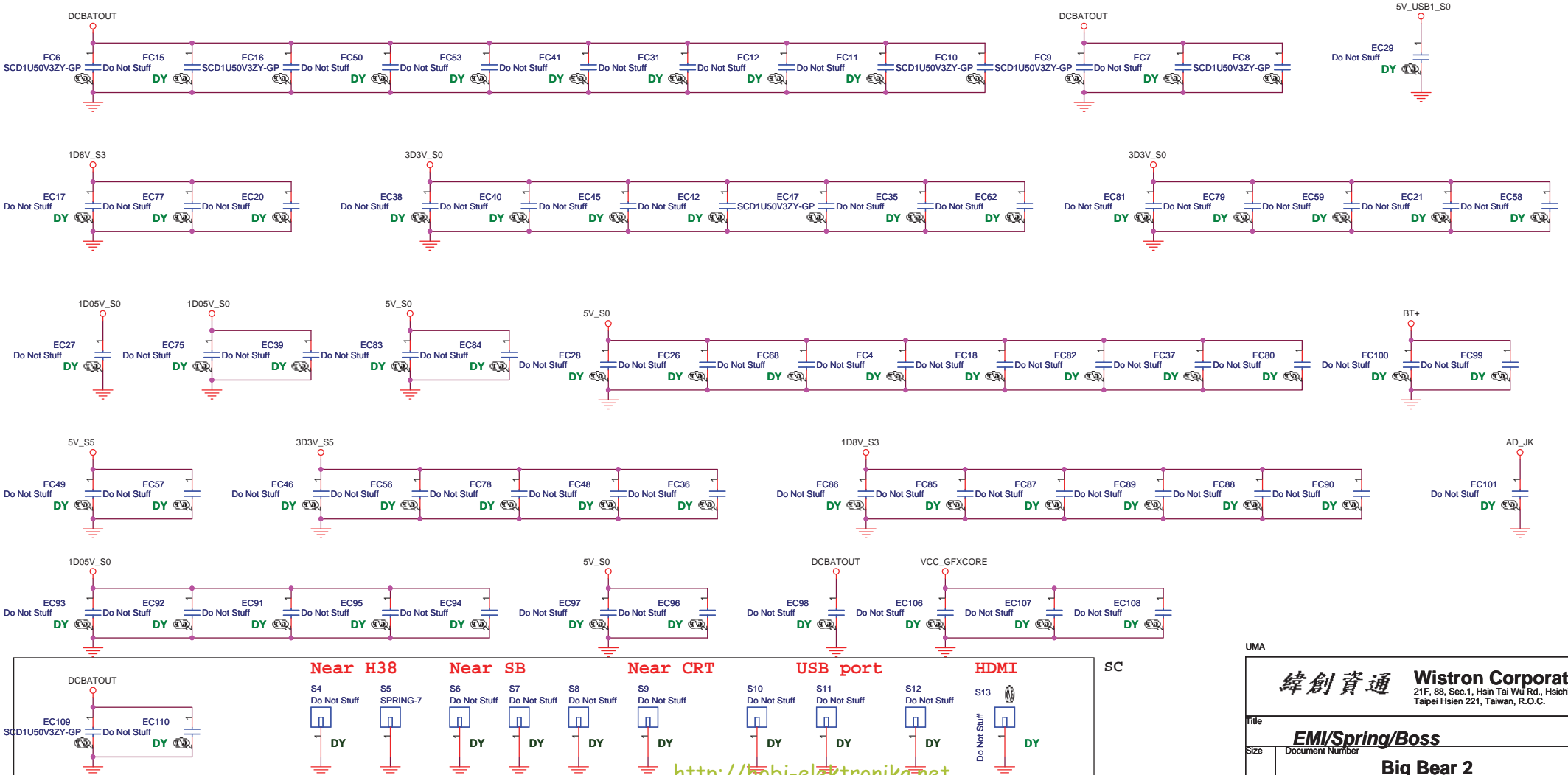
DIMM

Touch Pad

MXM SPRING



EMI



Near H38

Near SB

Near CRT

USB port

HDMI

SC

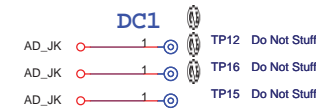
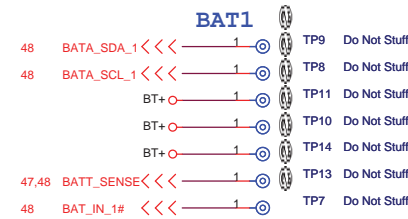
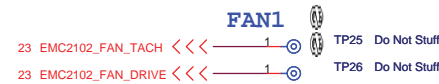
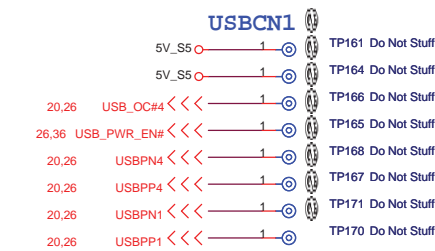
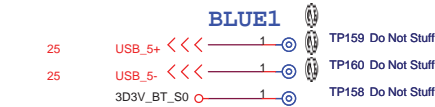
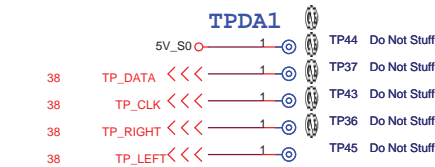
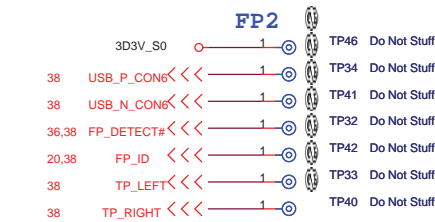
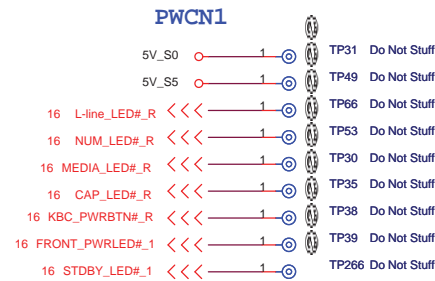
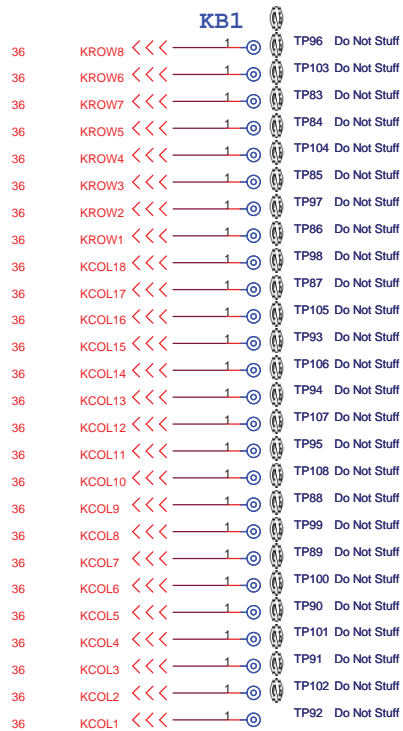
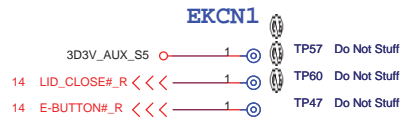
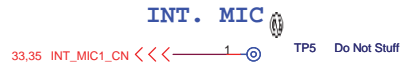
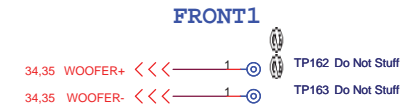
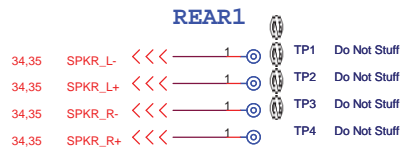
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Title			
AFTE			
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		50	of

Big Bear 2 Schematic EC Tracking Record LAB 0911 , 2008
EC #/ Page / Description / Part Affected

- EC SC01/20/Change R316 to 20R2F(For USB eye diagram)
- EC SC02/24/Swap net SATA_RXN5 SATA_RXP5
- EC SC03/29/Add C679 C680 for XF1(For IEEE common voltage channel D fail)
- EC SC04/33/Add RN95 RN104(vendor realtek request)
- EC SC05/36/Swap KBI1 pin definition

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Title

EC Tracking Record

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